DDR3 SDRAM Specification

January 2007

revision 0.1

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Table Contents

Revision History

Revision	Month	Year	History
0.0	November	2006	
0.1	January	2007	- Corrected AC parameter

1.0 DDR3 Unbuffered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
M378B6573EZ0-CE7/F7/F8/G8	512MB	64Mx64	64Mx8(K4B510846E-ZC##)*8	1	30mm
M391B6573EZ0-CE7/F7/F8/G8	512MB	64Mx72	64Mx8(K4B510846E-ZC##)*9	1	30mm
M378B2973EZ0-CE7/F7/F8/G8	1GB	128Mx64	64Mx8(K4B510846E-ZC##)*16	2	30mm
M391B2973EZ0-CE7/F7/F8/G8	1GB	128Mx72	64Mx8(K4B510846E-ZC##)*18	2	30mm

2.0 Key Features

Speed	DDR3-800		DDR3-1066			DDR3-1333		DDR3-1600		Unit
	5-5-5 E	6-6-6 F	6-6-6 E	7-7-7 F	8-8-8 G	8-8-8 G	9-9-9 H	9-9-9 H	10-10-10 J	
tCK(min)	2.5		1.875			1.5		1.25		ns
CAS Latency	5	6	6	7	8	8	9	9	10	tCK
tRCD(min)	12.5	15	11.25	13.125	15	12	13.5	11.25	12.5	ns
tRP(min)	12.5	15	11.25	13.125	15	12	13.5	11.25	12.5	ns
tRAS(min)	37.5	37.5	37.5	37.5	37.5	36	36	35	35	ns
tRC(min)	50	52.5	48.75	50.625	52.5	48	49.5	46.25	47.25	ns

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHzf_{CK} for 1600Mb/sec/pin
- 8 independent internal bank
- Programmable $\overline{CAS}$ Latency: (4),5,6,7,8,9,10,(11 for high density only)
- Posted $\overline{CAS}$
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency(CWL) = 5(DDR3-800), 6(DDR3-1066), 7(DDR3-1333), 8(DDR3-1600)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset
- 1066Mbps CL7 doesn’t have backward compatibility with 800Mbps CL5

3.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
64Mx8(512Mb) based Module	A0-A12	A0-A9	BA0-BA2	A10/AP

4.0 x64 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	$V_{REF}DQ$	121	V_{SS}	42	NC	162	$\overline{DQS}17$	82	DQ33	202	V_{SS}
2	V_{SS}	122	DQ4	43	NC	163	V_{SS}	83	V_{SS}	203	DM4,DQS13
3	DQ0	123	DQ5	44	V_{SS}	164	NC	84	$\overline{DQS}4$	204	$\overline{DQS}13$
4	DQ1	124	V_{SS}	45	NC	165	NC	85	DQS4	205	V_{SS}
5	V_{SS}	125	DM0,DQS9	46	NC	166	V_{SS}	86	V_{SS}	206	DQ38
6	$\overline{DQS}0$	126	NC,$\overline{DQS}9$	47	V_{SS}	167	TEST	87	DQ34	207	DQ39
7	DQS0	127	V_{SS}	48	NC	168	$\overline{Reset}$	88	DQ35	208	V_{SS}
8	V_{SS}	128	DQ6	KEY				89	V_{SS}	209	DQ44
9	DQ2	129	DQ7	49	NC	169	CKE1	90	DQ40	210	DQ45
10	DQ3	130	V_{SS}	50	CKE0	170	V_{DD}	91	DQ41	211	V_{SS}
11	V_{SS}	131	DQ12	51	V_{DD}	171	A15	92	V_{SS}	212	DM5,DQS14
12	DQ8	132	DQ13	52	BA2	172	A14	93	$\overline{DQS}5$	213	$\overline{DQS}14$
13	DQ9	133	V_{SS}	53	NC, $\overline{ERR\text{-}OUT}$[1]	173	V_{DD}	94	DQS5	214	V_{SS}
14	V_{SS}	134	DM1,DQS10	54	V_{DD}	174	A12	95	V_{SS}	215	DQ46
15	$\overline{DQS}1$	135	NC,$\overline{DQS}10$	55	A11	175	A9	96	DQ42	216	DQ47
16	DQS1	136	V_{SS}	56	A7	176	V_{DD}	97	DQ43	217	V_{SS}
17	V_{SS}	137	DQ14	57	V_{DD}	177	A8	98	V_{SS}	218	DQ52
18	DQ10	138	DQ15	58	A5	178	A6	99	DQ48	219	DQ53
19	DQ11	139	V_{SS}	59	A4	179	V_{DD}	100	DQ49	220	V_{SS}
20	V_{SS}	140	DQ20	60	V_{DD}	180	A3	101	V_{SS}	221	DM6,DQS15
21	DQ16	141	DQ21	61	A2	181	A1	102	$\overline{DQS}6$	222	$\overline{DQS}15$
22	DQ17	142	V_{SS}	62	V_{DD}	182	V_{DD}	103	DQS6	223	V_{SS}
23	V_{SS}	143	DQS11	63	CK1/NC	183	V_{DD}	104	V_{SS}	224	DQ54
24	$\overline{DQS}2$	144	$\overline{DQS}11$	64	$\overline{CK}1$/NC	184	CK0	105	DQ50	225	DQ55
25	DQS2	145	V_{SS}	65	V_{DD}	185	$\overline{CK}0$	106	DQ51	226	V_{SS}
26	V_{SS}	146	DQ22	66	V_{DD}	186	V_{DD}	107	V_{SS}	227	DQ60
27	DQ18	147	DQ23	67	$V_{REF}CA$	187	NF	108	DQ56	228	DQ61
28	DQ19	148	V_{SS}	68	NC,Par_In[1]	188	A0	109	DQ57	229	V_{SS}
29	V_{SS}	149	DQ28	69	V_{DD}	189	V_{DD}	110	V_{SS}	230	DM7,DQS16
30	DQ24	150	DQ29	70	A10	190	BA1/BA0	111	$\overline{DQS}7$	231	$\overline{DQS}16$
31	DQ25	151	V_{SS}	71	BA0/BA1	191	V_{DD}	112	DQS7	232	V_{SS}
32	V_{SS}	152	DM3,DQS12	72	V_{DD}	192	$\overline{RAS}$	113	V_{SS}	233	DQ62
33	$\overline{DQS}3$	153	$\overline{DQS}12$	73	$\overline{WE}$	193	$\overline{S}0$	114	DQ58	234	DQ63
34	DQS3	154	V_{SS}	74	$\overline{CAS}$	194	V_{DD}	115	DQ59	235	V_{SS}
35	V_{SS}	155	DQ30	75	V_{DD}	195	ODT0	116	V_{SS}	236	V_{DDSPD}
36	DQ26	156	DQ31	76	$\overline{S}1$	196	A13	117	SA0	237	SA1
37	DQ27	157	V_{SS}	77	ODT1	197	V_{DD}	118	SCL	238	SDA
38	V_{SS}	158	NC	78	V_{DD}	198	NF	119	V_{SS}	239	V_{SS}
39	NC	159	NC	79	RFU$\overline{SPD}$	199	V_{SS}	120	V_{TT}	240	V_{TT}
40	NC	160	V_{SS}	80	V_{SS}	200	DQ36				
41	V_{SS}	161	DM8,DQS17	81	DQ32	201	DQ37				

NC = No Connect; NF = No Function; NU = Not Usable; RFU = Reserved Future Use
1. Par_in and Err_out pins are intended for register control functions (Pins 53 and 68) and should not be connected anywhere on the UDIMM module.
2. NC pins should not be connected to anything, including bussing within the NC group.
3. Addresses A3-A8 can be mirrored or not mirrored. Please refer to Section 7.1 for more information on mirrored addresses.

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5.0 x72 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	$V_{REF}DQ$	121	V_{SS}	42	$\overline{DQS8}$	162	$\overline{DQS17}$	82	DQ33	202	V_{SS}
2	V_{SS}	122	DQ4	43	DQS8	163	V_{SS}	83	V_{SS}	203	DM4,DQS13
3	DQ0	123	DQ5	44	V_{SS}	164	CB6	84	$\overline{DQS4}$	204	$\overline{DQS13}$
4	DQ1	124	V_{SS}	45	CB2	165	CB7	85	DQS4	205	V_{SS}
5	V_{SS}	125	DM0,DQS9	46	CB3	166	V_{SS}	86	V_{SS}	206	DQ38
6	$\overline{DQS0}$	126	NC,$\overline{DQS9}$	47	V_{SS}	167	TEST	87	DQ34	207	DQ39
7	DQS0	127	V_{SS}	48	NC	168	$\overline{Reset}$	88	DQ35	208	V_{SS}
8	V_{SS}	128	DQ6	KEY				89	V_{SS}	209	DQ44
9	DQ2	129	DQ7	49	NC	169	CKE1	90	DQ40	210	DQ45
10	DQ3	130	V_{SS}	50	CKE0	170	V_{DD}	91	DQ41	211	V_{SS}
11	V_{SS}	131	DQ12	51	V_{DD}	171	A15	92	V_{SS}	212	DM5,DQS14
12	DQ8	132	DQ13	52	BA2	172	A14	93	$\overline{DQS5}$	213	$\overline{DQS14}$
13	DQ9	133	V_{SS}	53	NC, $\overline{ERR\text{-}OUT}$[1]	173	V_{DD}	94	DQS5	214	V_{SS}
14	V_{SS}	134	DM1,DQS10	54	V_{DD}	174	A12	95	V_{SS}	215	DQ46
15	$\overline{DQS1}$	135	NC,$\overline{DQS10}$	55	A11	175	A9	96	DQ42	216	DQ47
16	DQS1	136	V_{SS}	56	A7	176	V_{DD}	97	DQ43	217	V_{SS}
17	V_{SS}	137	DQ14	57	V_{DD}	177	A8	98	V_{SS}	218	DQ52
18	DQ10	138	DQ15	58	A5	178	A6	99	DQ48	219	DQ53
19	DQ11	139	V_{SS}	59	A4	179	V_{DD}	100	DQ49	220	V_{SS}
20	V_{SS}	140	DQ20	60	V_{DD}	180	A3	101	V_{SS}	221	DM6,DQS15
21	DQ16	141	DQ21	61	A2	181	A1	102	$\overline{DQS6}$	222	$\overline{DQS15}$
22	DQ17	142	V_{SS}	62	V_{DD}	182	V_{DD}	103	DQS6	223	V_{SS}
23	V_{SS}	143	DQS11	63	CK1/NC	183	V_{DD}	104	V_{SS}	224	DQ54
24	$\overline{DQS2}$	144	$\overline{DQS11}$	64	$\overline{CK1}$/NC	184	CK0	105	DQ50	225	DQ55
25	DQS2	145	V_{SS}	65	V_{DD}	185	$\overline{CK0}$	106	DQ51	226	V_{SS}
26	V_{SS}	146	DQ22	66	V_{DD}	186	V_{DD}	107	V_{SS}	227	DQ60
27	DQ18	147	DQ23	67	$V_{REF}CA$	187	NF	108	DQ56	228	DQ61
28	DQ19	148	V_{SS}	68	NC,Par_In[1]	188	A0	109	DQ57	229	V_{SS}
29	V_{SS}	149	DQ28	69	V_{DD}	189	V_{DD}	110	V_{SS}	230	DM7,DQS16
30	DQ24	150	DQ29	70	A10	190	BA1/BA0	111	$\overline{DQS7}$	231	$\overline{DQS16}$
31	DQ25	151	V_{SS}	71	BA0/BA1	191	V_{DD}	112	DQS7	232	V_{SS}
32	V_{SS}	152	DM3,DQS12	72	V_{DD}	192	$\overline{RAS}$	113	V_{SS}	233	DQ62
33	$\overline{DQS3}$	153	$\overline{DQS12}$	73	$\overline{WE}$	193	$\overline{S0}$	114	DQ58	234	DQ63
34	DQS3	154	V_{SS}	74	$\overline{CAS}$	194	V_{DD}	115	DQ59	235	V_{SS}
35	V_{SS}	155	DQ30	75	V_{DD}	195	ODT0	116	V_{SS}	236	V_{DDSPD}
36	DQ26	156	DQ31	76	$\overline{S1}$	196	A13	117	SA0	237	SA1
37	DQ27	157	V_{SS}	77	ODT1	197	V_{DD}	118	SCL	238	SDA
38	V_{SS}	158	CB4	78	V_{DD}	198	NF	119	V_{SS}	239	V_{SS}
39	CB0	159	CB5	79	RFU$\overline{SPD}$	199	V_{SS}	120	V_{TT}	240	V_{TT}
40	CB1	160	V_{SS}	80	V_{SS}	200	DQ36				
41	V_{SS}	161	DM8,DQS17	81	DQ32	201	DQ37				

NC = No Connect; NF = No Function; NU = Not Usable; RFU = Reserved Future Use
1. Par_in and Err_out pins are intended for register control functions (Pins 53 and 68) and should not be connected anywhere on the UDIMM module.
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3. Addresses A3-A8 can be mirrored or not mirrored. Please refer to Section 7.1 for more information on mirrored addresses.

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6.0 Pin Description

Pin Name	Description	Pin Name	Description
A0-A15	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0, BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0-SA1	I^2C serial address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}*	SDRAM core power supply
$\overline{WE}$	SDRAM wirte enable	V_{DDQ}*	SDRAM I/O Driver power supply
$\overline{S}$0, $\overline{S}$1	DIMM Rank Select Lines	V_{REF}DQ	SDRAM I/O reference supply
CKE0,CKE1	SDRAM clock enable lines	V_{REF}CA	SDRAM command/address reference supply
ODT0, ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0 - DQ63	DIMM memory data bus	V_{DD}SPD	Serial EEPROM positive power supply
CB0 - CB7	DIMM ECC check bits	NC	Spare Pins(no connect)
DQS0 - DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
$\overline{DQS}$0-$\overline{DQS}$8	SDRAM differential data strobes (negative line of differential pair)	$\overline{RESET}$	Set DRAMs Known State
DM(0-8)	SDRAM data masks/high data strobes (x8-based DIMMs)	NF	No function
CK0, CK1	SDRAM clocks (positive line of differential pair)	V_{TT}	SDRAM I/O termination supply
$\overline{CK}$0, $\overline{CK}$1	SDRAM clocks (negative line of differential pair)	RFU	Reserved for future use

*The VDD and VDDQ pins are tied common to a single power-plane on these desigus.

7.0 Input/Output Functional Description

Symbol	Type	Function
CK0-CK1 $\overline{CK0}$-$\overline{CK1}$	SSTL	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is reference to the crossing of CK and $\overline{CK}$ (Both directions of crossing)
CKE0-CKE1	SSTL	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode
$\overline{S}$0-$\overline{S}$1	SSTL	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (ALONG WITH $\overline{S}$) define the command being entered.
ODT0-ODT1	SSTL	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V_{REF}DQ	Supply	Reference voltage for SSTL 15 I/O inputs.
V_{REF}CA	Supply	Reference voltage for SSTL 15 command/address inputs.
V_{DDQ}	Supply	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0-BA2	SSTL	Selects which SDRAM bank of eight is activated.
A0-A15	SSTL	During a Bank Activate command cycle, Address input defines the row address (RA0-RA15) During a Read or Write command cycle, Address input defines the colum address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a pre-charge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge.
DQ0-DQ63 CB0-CB7	SSTL	Data and Check Bit Input/Output pins.
DM0-DM8	SSTL	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply	Power and ground for DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0-DQS8 $\overline{DQS0}$-$\overline{DQS8}$	SSTL	Data strobe for input and output data. For raw cards using x16 orginized DRAMs, Pins DQ0-7 are associated with the LDQS and $\overline{LDQS}$ pins and Pins DQ8-15 are associated with UDQS and $\overline{UDQS}$ pins.
SA0-SA1	-	These signals and tied at the system planar to either V_{SS} or V_{DD}SPD to configure the serial SPD EERPOM address range.
SDA	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DD}SPD to act as a pullup on the system board.
SCL	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DD}SPD to act as a pullup on the system board.
V_{DD} SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 3.0V to 3.6V.
$\overline{RESET}$	-	Active Low Asynchronous Reset : Reset is active when $\overline{RESET}$ is Low, and inactive when $\overline{RESET}$ is High. $\overline{RESET}$ must be High during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.

7.1 Address Mirroring Feature

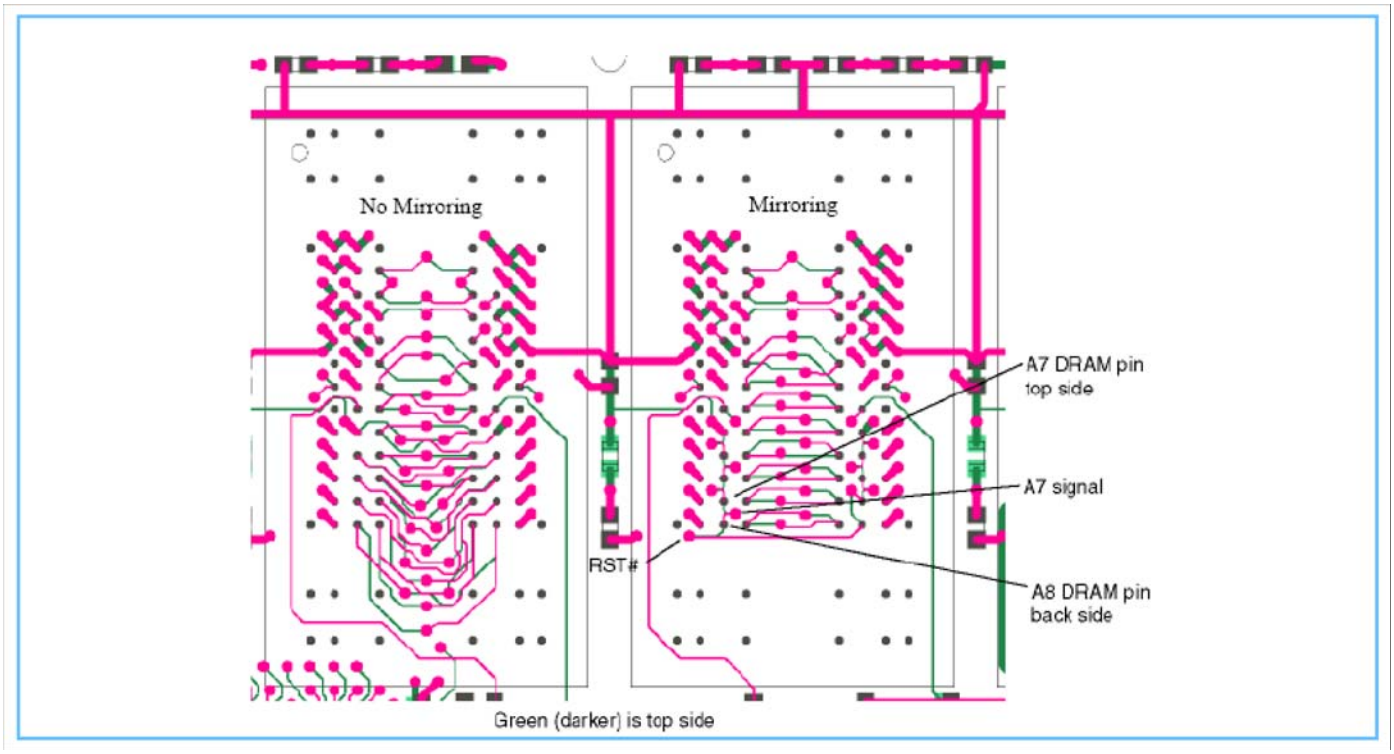
There is a via grid located under the DRAMs for wiring the CA signals (address, bank address, command, and control lines) to the DRAM pins. The length of the traces from the vias to the DRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces. The pins on the DRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 DRAM pins are wired straight, with no mismatch between the connector pin assignment and the DRAM pin assignment. Some of the Rank 1 DRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

7.1.1 DRAM Pin Wiring for Mirroring

Connector Pin	DRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

Figure 7.1.1 illustrates the wiring in both the mirrored and non-mirrored case. The lengths of the traces to the DRAM pins, is obviously shorter. The via grid is smaller as well.

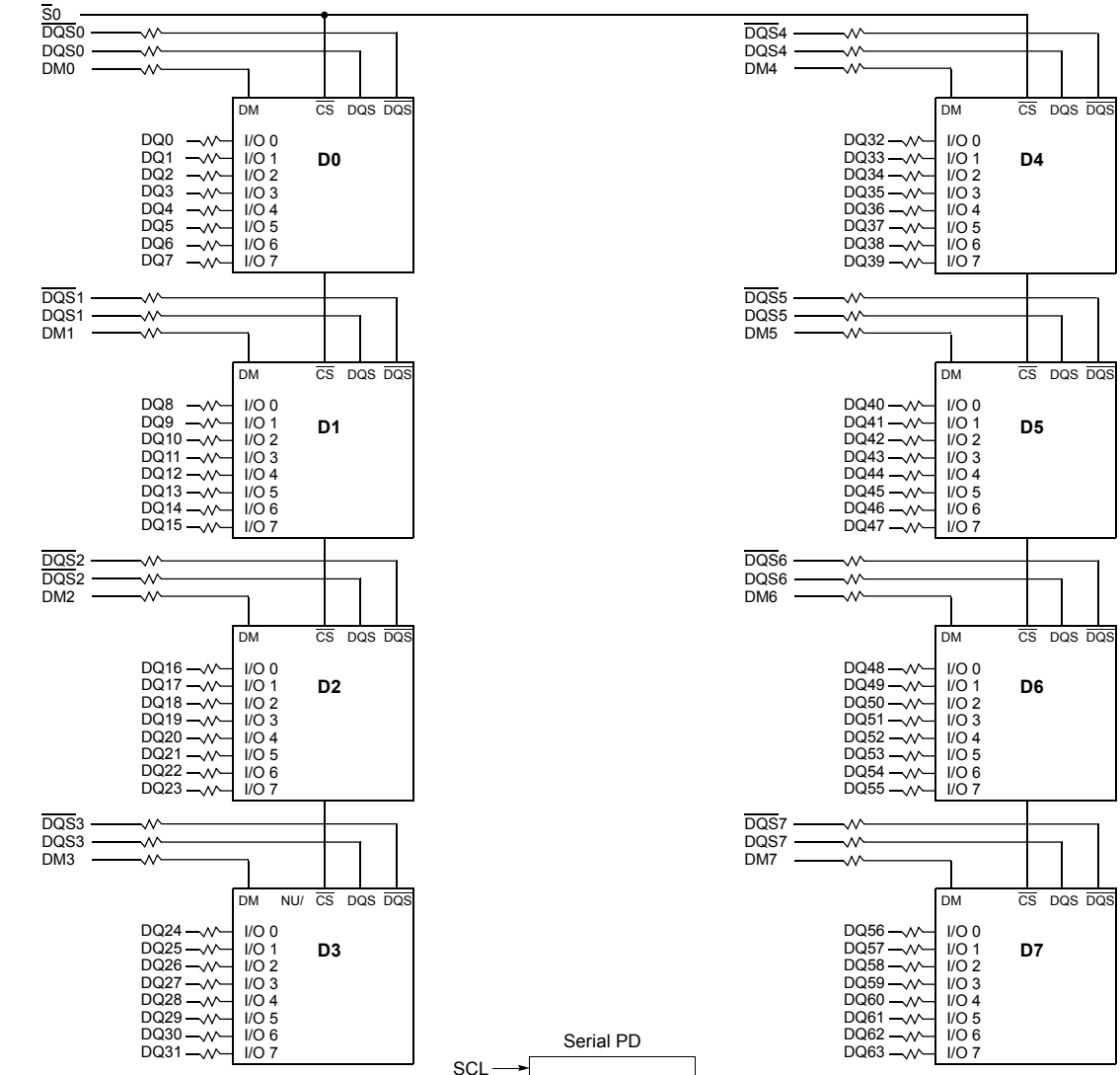
Figure 7.1.1 - Wiring Differences for Mirrored and Non-Mirrored Addresses-No Mirroring Mirroring

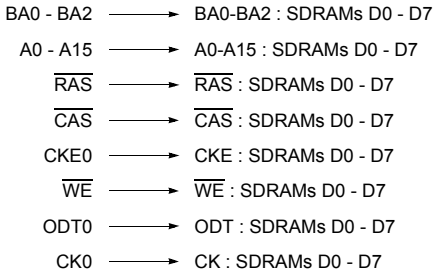


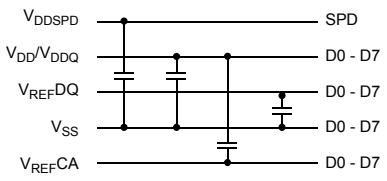
Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. This requires a fewrules. Mirroring is done on 2 rank modules and can only be done on the second rank. There is not a requirement that the second rank be mirrored. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR3 UDIMM SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank.

8.0 Functional Block Diagram:

8.1 512MB, 64Mx64 Module(Populated as 1 rank of x8 DDR3 SDRAMs)



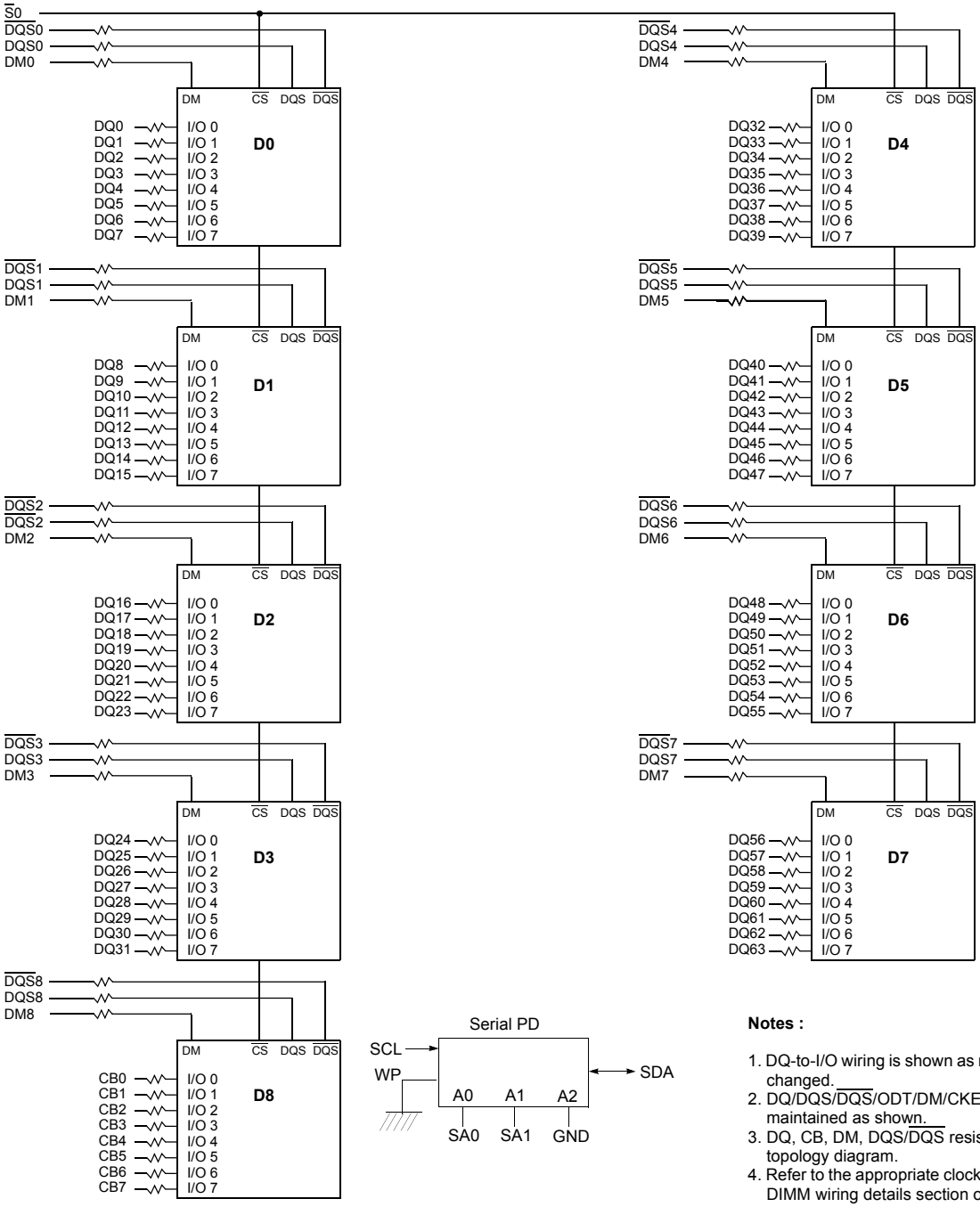




Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.

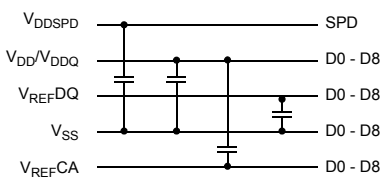
8.2 512MB, 64Mx72 ECC Module(Populated as 1 rank of x8 DDR3 SDRAMs)



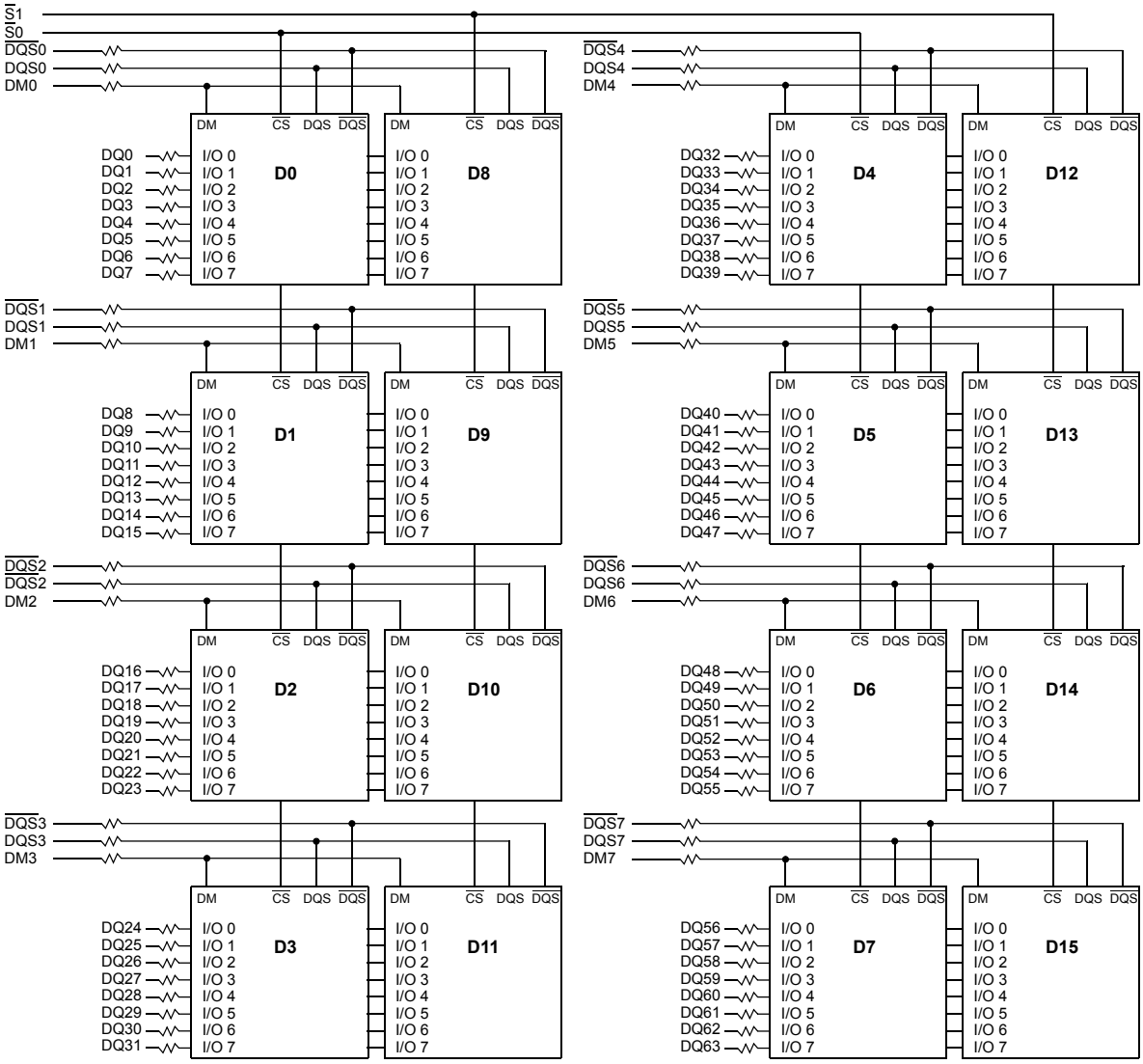
Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, CB, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.

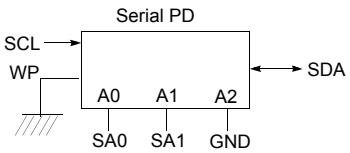
BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D8
A0 - A15 → A0-A15 : SDRAMs D0 - D8
$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D8
$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D8
CKE0 → CKE : SDRAMs D0 - D8
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D8
ODT0 → ODT : SDRAMs D0 - D8
CK0 → CK : SDRAMs D0 - D8

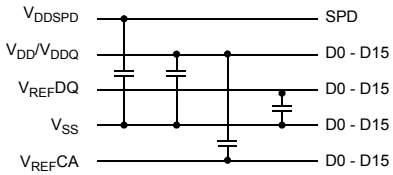


8.3 1GB, 128Mx64 Module(Populated as 2 ranks of x8 DDR3 SDRAMs)



BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D15
A0 - A15 → A0-A15 : SDRAMs D0 - D15
CKE1 → CKE : SDRAMs D8 - D15
CKE0 → CKE : SDRAMs D0 - D7
$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D15
$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D15
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D15
ODT0 → ODT : SDRAMs D0 - D7
ODT1 → ODT : SDRAMs D8 - D15
CK0 → CK : SDRAMs D0 - D7
CK1 → CK : SDRAMs D8 - D15

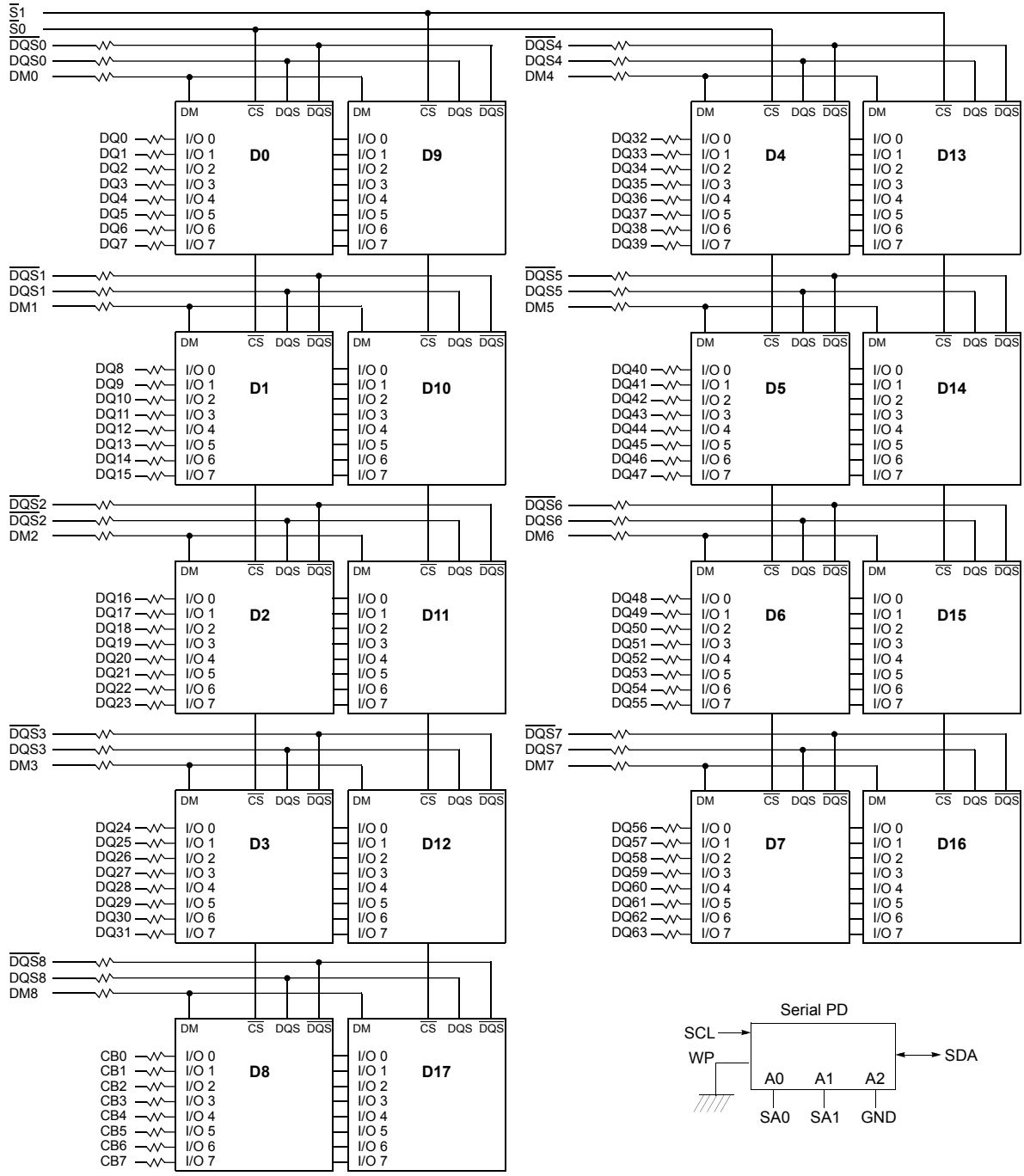




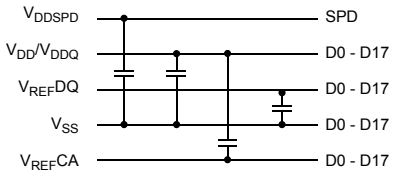
Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.

8.4 1GB, 128Mx72 ECC Module(Populated as 2 ranks of x8 DDR3 SDRAMs)



BA0 - BA2 → BA0-BA2 : SDRAMs D0 - D17
A0 - A15 → A0-A15 : SDRAMs D0 - D17
CKE1 → CKE : SDRAMs D9 - D17
CKE0 → CKE : SDRAMs D0 - D8
$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D17
$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D17
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D17
ODT0 → ODT : SDRAMs D0 - D8
ODT1 → ODT : SDRAMs D9 - D17
CK0 → CK : SDRAMs D0 - D8
CK1 → CK : SDRAMs D9 - D17



Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, CB, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.

9.0 Absolute Maximum Ratings

9.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

9.2 DRAM Component Operating Temperature Range

Symbol	Parameter	rating	Unit	Notes
TOPER	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range (Optional)	85 to 95	°C	1,3

Note :

1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9us. (This double refresh requirement may not apply for some devices.)

b) If Self-Refresh operation is required in the extended Temperature Range. then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6=0_b and MR2 A7 = 1_b) or enable the Auto Self-Refresh mode (MR2 A6 = 1_b and MR2 A7 = 0_b).

10.0 AC & DC Operating Conditions

10.1 Recommended DC Operating Conditions (SSTL - 15)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2
$V_{REFDQ(DC)}$	I/O Reference Voltage(DQ)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
$V_{REFCA(DC)}$	I/O Reference Voltage(CMD/Add)	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
VTT	Termination Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	4

Note :

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The ac peak niuse on VREF may not allow VREF to deviate from $V_{REF(DC)}$ by more than +/- 1% VDD (for reference : approx. +/- 15mV)
4. For reference : approx. VDD/2 +/- 15mV

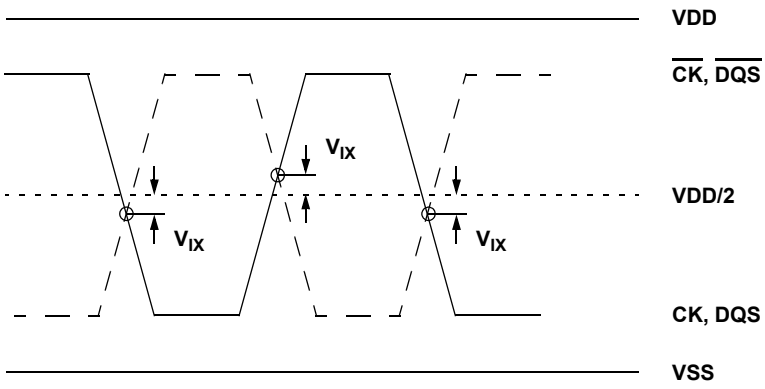
10.2 Input DC/AC Logic Level (SSTL_15)

Symbol	Parameter	Speed (Mtps)	Min.	Max.	Unit	Notes
V_{IH}(dc)	dc input logic high	800	VREF + 100	TBD	mV	1
		1066	VREF + 100			
		1333	VREF + 100			
		1600	VREF + 100			
V_{IL}(dc)	dc input logic low	800	TBD	VREF - 100	mV	1
		1066		VREF - 100		
		1333		VREF - 100		
		1600		VREF - 100		
V_{IH}(ac)	ac input logic high	800	VREF + 175	-	mV	1,2
		1066	VREF + 175			
		1333	VREF + 175			
		1600	VREF + 175			
V_{IL}(ac)	ac input logic low	800	-	VREF - 175	mV	1,2
		1066		VREF - 175		
		1333		VREF - 175		
		1600		VREF - 175		
$V_{REFDQ(DC)}$	I/O Reference Voltage(DQ)	800/1066/1333/1600	0.49*VDDQ	0.51*VDDQ	V	3,4
$V_{REFCA(DC)}$	I/O Reference Voltage(CMD/Add)	800/1066/1333/1600	0.49*VDDQ	0.51*VDDQ	V	3,4
VTT	Termination Voltage	800/1066/1333/1600	0.49*VDDQ	0.51*VDDQ	V	3,4

Note :
1. For DQ and DM, $V_{REF} = V_{REFDQ}$. For input only pins except RESET, or $V_{REF} = V_{REFCA}$
2. See X.X "Overshoot and Undershoot specifications" on page xxx
3. The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF(DC)}$ by more than +/1 1% VDD (for reference : approx. +/- 15mV)
4. For reference : approx. VDD/2 +/- 15mV

10.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



Cross point voltage for differential input signals (CK, DQS)

Symbol	Description	DDR3-800/1066		DDR3-1333/1600		Unit	Notes
		Min	Max	Min	Max		
VIX	Differential input Cross point voltage relative to VDD/s	-150	150	-150	150	mV	

10.4 Slew rate definition

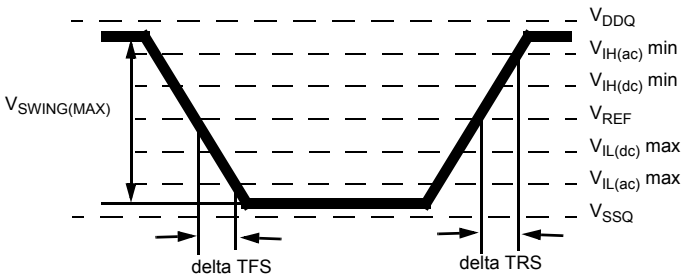
10.4.1 Slew rate definition for Single-ended signals

Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)
Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

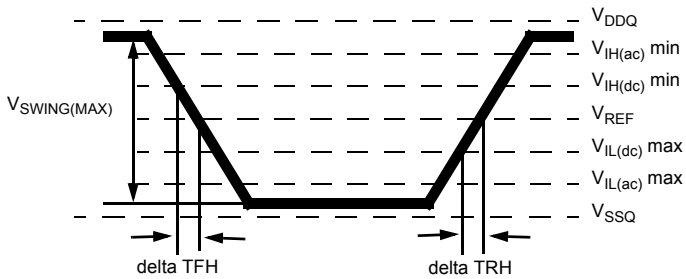
Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)
Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef

Description	Measured		Defined by	Applicable for
	From	To		
Input slew rate for rising edge	Vref	Vih(AC)min	Vih(AC)min-Vref / Delta TRS	Setup (tIS,tDS)
Input slew rate for falling edge	Vref	Vil(AC)max	Vref-Vil(AC)max / Delta TFS	
Input slew rate for rising edge	Vil(DC)max	Vref	Vref-Vil(DC)max / Delta TFH	Hold (tIH,tDH)
Input slew rate for falling edge	Vih(DC)min	Vref	Vih(DC)min-Vref / Delta TRH	

Notes : This nominal slew rate applies for linear signal waveforms.



< Figure : Input slew rate for setup>



< Figure : Input slew rate for Hold>

10.5 Slew rate definition for Differential signals

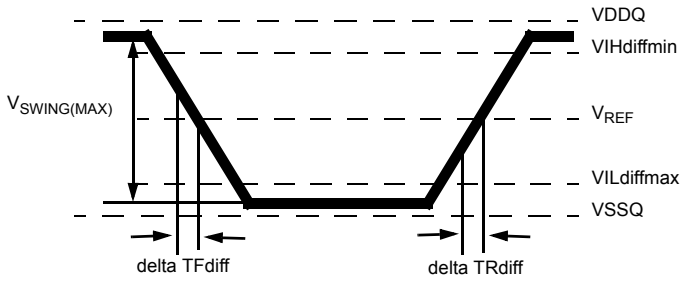
Differential DC and AC input levels

Symbol	Description	DDR3-800/1066		DDR3-1333/1600		Unit	Notes
		Min	Max	Min	Max		
VIHdiff	Differential input logic high	+ 200	TBD	+ 200	TBD	mV	1
VILdiff	Differential input logic low	TBD	- 200	TBD	- 200		

Note1: The TBD might be changed based on overshoot undershoot values

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	VIHdiffmin - VILdiffmax / Delta TRdiff
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	VIHdiffmin - VILdiffmax / Delta TFdiff

The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be monothonic between these thresholds



< Figure : Differential input slew rate definition for DQS,$\overline{DQS}$ and CK,$\overline{CK}$>

10.6 Output DC and AC output levels

Single Ended DC and AC output levels

Symbol	Parameter	DDR3-800/1066/1333/1600	Units	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

Note :

1. The swing of +/-0.1xVDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40ohms and an effective test load of 25ohms to Vtt=VDDQ/2.

10.6.1 Differential DC and AC output levels

Symbol	Parameter	DDR3-800/1066/1333/1600	Units	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+0.2 x VDDQ	V	1
$V_{OLdiff(DC)}$	AC differential output low measurement level (for output SR)	-0.2 x VDDQ	V	1

Note :

1. The swing of +/-0.2xVDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40ohms and an effective test load of 25ohms to Vtt=VDDQ/2.

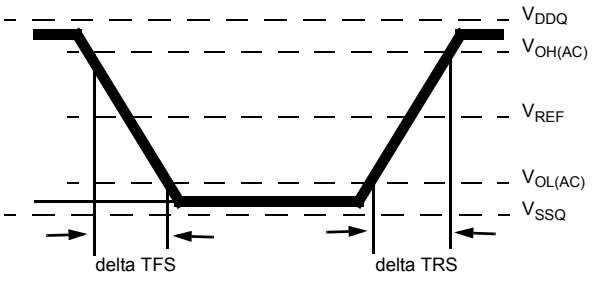
10.6.2 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in the below Table and figure.

Output slew rate is verified by design and characterization, but may not be subject to production test.

Description	Measured		Defined by	Applicable for
	From	To		
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{Delta\ TRse}$	
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{Delta\ TFse}$	

Parameters	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	2.5	5	2.5	5	2.5	5	TBD	5	V/ns



< Figure : Input slew rate for setup>

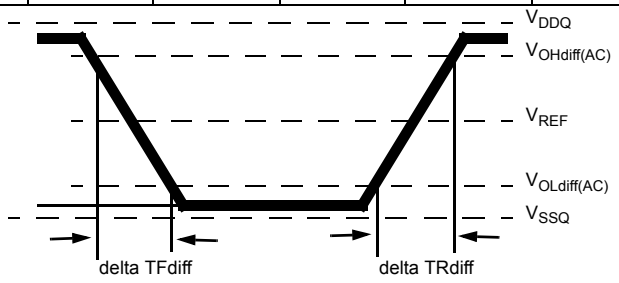
10.6.3 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in the below Table and figure.

Output slew rate is verified by design and characterization, but may not be subject to production test

Description	Measured		Defined by	Applicable for
	From	To		
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TRdiff	
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) / Delta TFdiff	

Parameters	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	5	10	5	10	5	10	TBD	10	V/ns



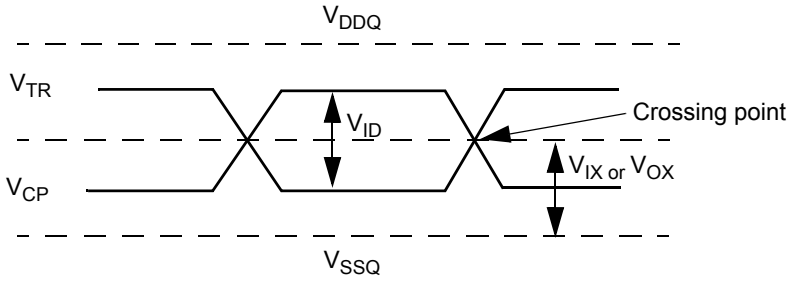
< Figure : Input slew rate for setup>

10.7 Default driver characteristics

Symbol	Parameter/Condition		Min.	Max.	Units	Notes
VID (ac)	ac differential input voltage	800 ~ 1066 MTS	400	VDDQ + 0.6	V	1
		1333 ~ 1600 MTS	350			
VIX (ac)	ac differential cross point voltage		0.5 * VDDQ - 0.175	0.5 * VDDQ + 0.175	V	2
SLEW_CK	Differential input slew rate(min) for CK/CK		2		V/ns	3
SLEW_DQSin	Differential slew rate(min) for DQS/DQS		2		V/ns	3
VOX (ac)	Differential ac output cross point voltage		0.5*Vddq - tbd	0.5*Vddq + tbd	V	4
SOUT_diff	Differential output slew rate(min) for DQS/DQS		5	tbd	V/ns	
Delta SOUT_diff	Mismatch of output slew rate between DQS and DQS			0.25	V/ns	

Note :

1. VID (ac) specifies the input differential voltage IVTR - VCPI required for switching, where VTR is the true input signal (such as CK, DQS, DQSL or DQSU) and VCP is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$). The minimum value is equal to VIH(ac) - VIL(ac).
2. The typical value of VIX(ac) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(ac) is expected to track variations in VDDQ. VIX(ac) indicates the voltage at which differential input signals must cross.
3. This differential input slew rate is measured at DDR3 SDRAM pins and used as DDR3 SDRAM test condition.
4. The typical value of VOX(ac) is expected to be about 0.5 * VDDQ of the transmitting device and VOX(ac) is expected to track variations in VDDQ. VOX(ac) indicates the voltage at which differential onput signals must cross.



< Differential signal levels >

10.8 Default driver characteristics

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Conditions	Max	Units	Notes
IDD0	**Operating one bank active-precharge current**; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RAS} = $t_{RASmin(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC\ (IDD)}$, t_{RAS} = $t_{RASmin(IDD)}$, t_{RCD} = $t_{RCD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	TBD	mA	
IDD2P	**Precharge power-down current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	mA	
IDD2N	**Precharge standby current**; All banks idle; t_{CK} = $t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD3P	**Active power-down current**; All banks open; t_{CK} = $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	mA	
IDD3N	**Active standby current**; All banks open; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RAS-max(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;Data bus inputs are SWITCHING	TBD	mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; t_{CK} = $t_{CK(IDD)}$, t_{RAS} = $t_{RASmax(IDD)}$, t_{RP} = $t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	TBD	mA	
IDD5B	**Burst refresh current**; t_{CK} = $t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	mA	
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	TBD	mA	
IDD6ET	**Extended Temperature Range Self-Refresh Current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1	TBD	mA	
IDD6TC	**Auto Self-Refresh Current**: CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable when ASR is enabled by MR2 setting A6=1 and A7=0	TBD	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RRD} = $t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	TBD	mA	

10.8.1 Default driver characteristics

Within the tables provided further down, an overview about the IDD measurement conditions is provided as follows:

Table 1 Overview of Tables providing IDD Measurement Conditions and DRAM Behavior

Table number	Measurement Conditions
Table 5	IDD0 and IDD1
Table 6	IDD2N, IDD2Q, IDD2P(0), IDD2P(1)
Table 7	IDD3N and IDD3P
Table 8	IDD4R, IDD4W, IDD7
Table 10	IDD5B
Table 11	IDD6, IDD6ET

Within the tables about IDD measurement conditions, the following definitions are used:

• LOW is defined as V_{IN} <= V_{ILAC}(max.); HIGH is defined as V_{IN} >= V_{IHAC}(min.);
• STABLE is defined as inputs are stable at a HIGH or LOW level
• FLOATING is defined as inputs are V_{REF} = V_{DDQ} / 2
• SWITCHING is defined as described in the following 2 tables.

Table 2 Definition of SWITCHING for Address and Command Input Signals

SWITCHING for Address (row, column) and Command Signals ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) is defined as:	
Address (row, column):	If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value (e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax ..... please see each IDDx definition for details)
Bank address:	If not otherwise mentioned the bank addresses should be switched like the row/ column addresses - please see each IDDx definition for details
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$):	Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, LOW, LOW, LOW} Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, HIGH,HIGH,HIGH} Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ ... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R) the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command. See each IDDx definition for details and figures 1,2,3 as examples.

Table 3 Definition of SWITCHING for Data (DQ)

SWITCHING for Data (DQ) is defined as	
Data (DQ)	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details. See figures 1,2,3 as examples.
Data Masking (DM)	NO Switching; DM must be driven LOW all the time

Table 4 For IDD testing the following parameters are utilized.

Parameter Bin		DDR3 800		DDR3 1066			DDR3 1333			DDR3 1600			Unit
		5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	8-8-8	9-9-9	101010	
t_{CKmin}(IDD)		2.5		1.875			1.5			1.25			ns
CL(IDD)		5	6	6	7	8	7	8	9	8	9	10	
t_{RCDmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
t_{RCmin}(IDD)		50	52.5	48.75	50.63	52.50	46.5	48	49.5	45	46.25	47.25	ns
t_{RASmin}(IDD)		37.5	37.5	37.5	37.5	37.5	36	36	36	35	35	35	ns
t_{RPmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
t_{FAW}(IDD)	x4/x8	40	40	37.5	37.5	37.5	30	30	30	30	30	30	ns
	x16	50	50	50	50	50	45	45	45	40	40	40	ns
t_{RRD}(IDD)	x4/x8	10	10	7.5	7.5	7.5	6.0	6.0	6.0	6.0	6.0	6.0	ns
	x16	10	10	10	10	10	7.5	7.5	7.5	7.5	7.5	7.5	ns
t_{RFC}(IDD) - 512Mb		90	90	90	90	90	90	90	90	90	90	90	ns
t_{RFC}(IDD) - 1 Gb		110	110	110	110	110	110	110	110	110	110	110	ns
t_{RFC}(IDD) - 2 Gb		160	160	160	160	160	160	160	160	160	160	160	ns
t_{RFC}(IDD) - 4 Gb		300	300	300	300	300	300	300	300	300	300	300	ns

The following conditions apply:
1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric test conditions.
3. IDD parameters are specified with ODT and output buffer disabled (MR1 Bit A12).

Table 5 IDD Measurement Conditions for IDD0 and IDD1

Current	IDD0	IDD1
Name	Operating Current 0 -> One Bank Activate -> Precharge	Operating Current 1 -> One Bank Activate -> Read -> Precharge
Measurement Condition		
Timing Diagram Example		Figure 1
CKE	HIGH	HIGH
External Clock	on	on
t_{CK}	t_{CK}min(IDD)	t_{CK}min(IDD)
t_{RC}	t_{RC}min(IDD)	t_{RC}min(IDD)
t_{RAS}	t_{RAS}min(IDD)	t_{RAS}min(IDD)
t_{RCD}	n.a.	t_{RCD}min(IDD)
t_{RRD}	n.a.	n.a.
CL	n.a.	CL(IDD)
AL	n.a.	0
$\overline{CS}$	HIGH between. Activate and Precharge Commands	HIGH between Activate, Read and Precharge
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 2; only exceptions are Activate and Precharge commands; example of IDD0 pattern: A0 D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ **P0** (DDR3-800: tRAS = 37.5ns between (A)ctivate and (P)recharge to bank 0 ; Definition of D and D: see Table 2)	SWITCHING as described in Table 2; only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern: A0 D $\overline{D}$ $\overline{D}$ D R0 D $\overline{D}$ $\overline{D}$ DD $\overline{D}$ $\overline{D}$ DD $\overline{D}$ **P0** (DDR3-800 -555: tRCD = 12.5ns between (A)ctivate and (R)ead to bank 0 ; Definition of D and D: see Table 2)
Row, Column Addresses	Row addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	Row addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!
Bank Addresses	bank address is fixed (bank 0)	bank address is fixed (bank 0)
Data I/O	SWITCHING as described in Table 3	Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1". When there is no read data burst from DRAM the DQ I/O should be FLOATING.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	one ACT-PRE loop	one ACT-RD-PRE loop
Idle banks	all other	all other
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.

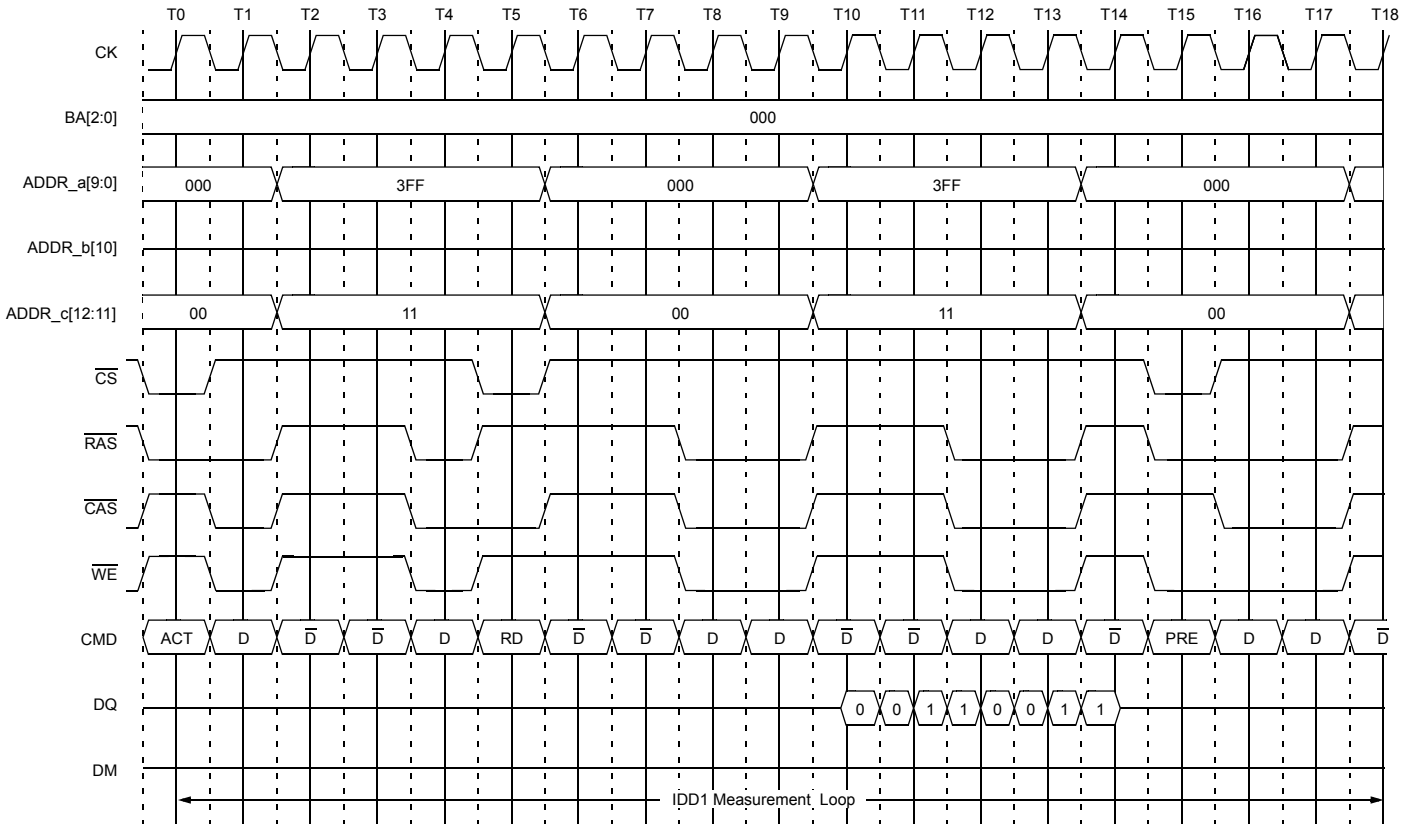


Figure 1

IDD1 Example (DDR3-800-555, 512Mb x8): Data DQ is shown but the output buffer should be switched off (per MR1 Bit A12 ="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

Table 6 IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

Current	IDD2N	IDD2P(1) a	IDD2P(0)	IDD2Q
Name	Precharge Standby Current	Precharge Power Down Current Fast Exit - MRS A12 Bit = 1	Precharge Power Down Current Slow Exit - MRS A12 Bit = 0	Precharge Quiet Standby Current
Measurement Condition				
Timing Diagram Example	Figure 2			
CKE	HIGH	LOW	LOW	LOW
External Clock	on	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	n.a.	n.a.
t_{RAS}	n.a.	n.a.	n.a.	n.a.
t_{RCD}	n.a.	n.a.	n.a.	n.a.
t_{RRD}	n.a.	n.a.	n.a.	n.a.
CL	n.a.	n.a.	n.a.	n.a.
AL	n.a.	n.a.	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE	HIGH	STABLE
Bank Address, Row Addr. and Command Inputs	SWITCHING as described in Table 2	STABLE	STABLE	STABLE
Data inputs	SWITCHING	FLOATING	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.	n.a.	n.a.
Active banks	none	none	none	none
Idle banks	all	all	all	all
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	Fast Exit / 1 (any valid command after tXP[b])	Slow Exit / 0 Slow exit (RD and ODT commands must satisfy tXPDLL-AL)	n.a.

a. In DDR3 the MRS Bit 12 defines DLL on/off behavior ONLY for precharge power down. There are 2 different Precharge Power Down states possible : one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).

b. Because it is an exit after precharge power down the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh.

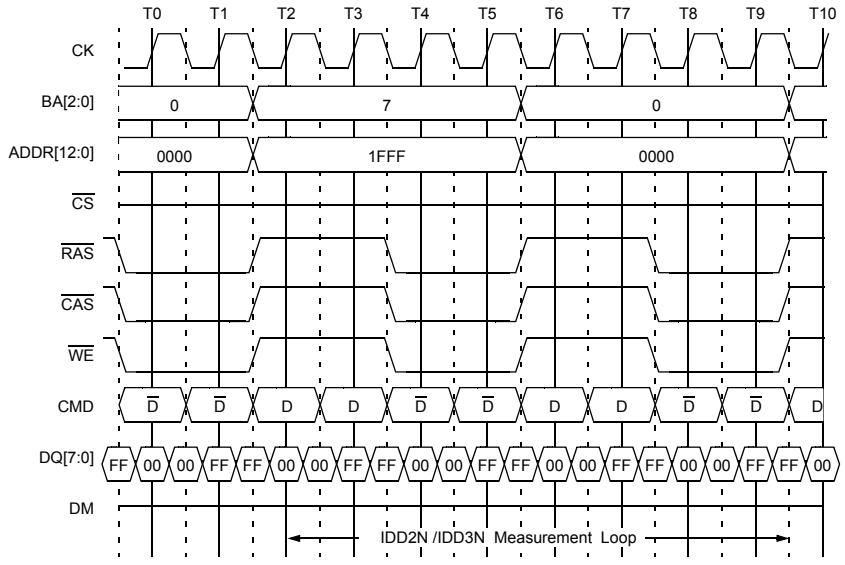


Figure2
IDD2N /IDD3N Example (DDR3-800-555, 512Mb X8)

Table 7 IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

Current	IDD3N	IDD3P
Name	Active Standby Current	Active Power-Down Current[a] Always Fast Exit
Measurement Condition		
Timing Diagram Example	Figure 2	
CKE	HIGH	LOW
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE
Addr. and cmd Inputs	SWITCHING as described in Table 2	STABLE
Data inputs	SWITCHING as described in Table 3	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all	all
Idle banks	none	none
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	n.a. (Active Power Down Mode is always "Fast Exit" with DLL on

a. DDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MRS bit 12 will not be used for active power down. Instead bit 12 will be used to switch between 2 different precharge power down modes.

Table 8 IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	IDD4R	IDD4W	IDD7
Name	Operating Current Burst Read	Operating Current Burst Write	All Bank Interleave Read Current
Measurement Condition			
Timing Diagram Example	Figure 3		
CKE	HIGH	HIGH	HIGH
External Clock	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	t_{RCmin}(IDD)
t_{RAS}	n.a.	n.a.	t_{RASmin}(IDD)
t_{RCD}	n.a.	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.	t_{RRDmin}(IDD)
CL	CL(IDD)	CL(IDD)	CL(IDD)
AL	0	0	t_{RCDmin}-1t_{CK}
$\overline{CS}$	HIGH btw. valid cmds	HIGH btw. valid cmds	HIGH btw. valid cmds
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 2; exceptions are Read commands => IDD4R Pattern: R0D$\overline{DD}$R1D$\overline{DD}$R2D$\overline{DD}$R3D$\overline{DD}$R4 ..... Rx = Read from bank x; Definition of D and D: see Table 2	SWITCHING as described in Table 2; exceptions are Write commands => IDD4W Pattern: W0D$\overline{DD}$W1D$\overline{DD}$W2D$\overline{DD}$W3D$\overline{DD}$ W4 ... Wx = Write to bank x; Definition of D and D: see Table 2	For patterns see Table 9
Row, Column Addresses	column addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	column addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	STABLE during DESELECTs
Bank Addresses	bank address cycling (0 ->1 -> 2 -> 3 ...)	bank address cycling (0 ->1 -> 2 -> 3 ...)	bank address cycling (0 ->1 -> 2 -> 3 ...), see pattern in Table 9
DQ I/O	Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1".	Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle. DM is low all the time.	Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1".
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	all	all	all
Idle banks	none	none	none
Precharge Power Down Mode / Mode Register Bit	n.a.	n.a.	n.a.

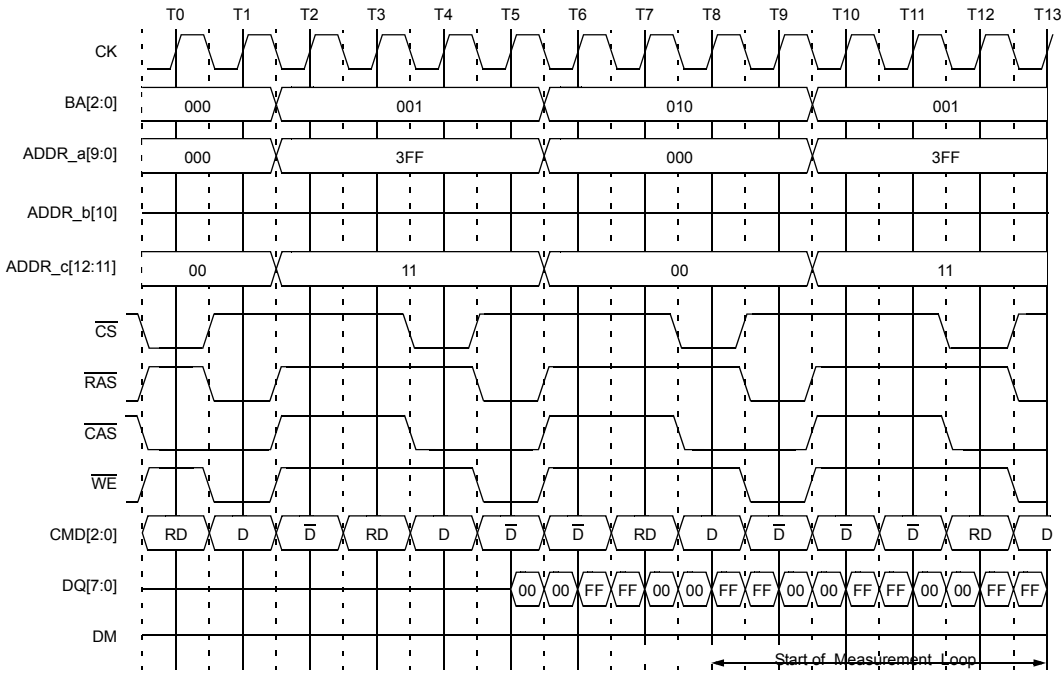


Figure3
IDD4R Example (DDR3-800-555, 512Mb x8): data DQ is shown but the output buffer should be switched off (per MR1 Bit A12=°±1°±) to achieve Iout = 0mA. Address inputs are split into 3 parts.

Table 9 IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

Speed	Bin	Org.	tFAW	tFAW	tRRD	tRRD	IDD7 Pattern[a]
Mb/s			[ns]	[CLK]	[ns]	[CLK]	
800	all	x4/x8	40	16	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7D D
	all	x16	50	20	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD D D D D A4 RA4 D D A5 RA5 D D A6 RA6 DD A7 RA7 D D D D D D
1066	all	x4/x8	37.5	20	7.5	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD D D D D A4 RA4 D D A5 RA5 D D A6 RA6 DD A7 RA7 D D D D D D
	all	x16	50	27	10	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D D A4 RA4 D D D D A5RA5 D D D D A6 RA6 D D D D A7 RA7 D D D DD D D
1333	all	x4/x8	30	20	6	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 DD D D D D A4 RA4 D D A5 RA5 D D A6 RA6 DD A7 RA7 D D D D D D
	all	x16	45	30	7.5	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3RA3 D D D D D D D D D D D D D A4 RA4 D D DA5 RA5 D D D A6 RA6 D D D A7 RA7 D D D DD D D D D D D D D
1600	all	x4/x8	30	24	6	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3RA3 D D D D D D D A4 RA4 D D D A5 RA5 D DD A6 RA6 D D D A7 RA7 D D D D D D D
	all	x16	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D D D D D D A4 RA4D D D D A5 RA5 D D D D A6 RA6 D D D D A7RA7 D D D D D D D D D D D D

a. A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

Table 10 IDD Measurement Conditions for IDD5B

Current	IDD5B
Name	Burst Refresh Current
Measurement Condition	
CKE	HIGH
External Clock	on
t_{CK}	t_{CKmin}(IDD)
t_{RC}	n.a.
t_{RAS}	n.a.
t_{RCD}	n.a.
t_{RRD}	n.a.
t_{RFC}	t_{RFCmin}(IDD)
CL	n.a.
AL	n.a.
$\overline{CS}$	HIGH btw. valid cmds
Addr. and cmd Inputs	SWITCHING
Data inputs	SWITCHING
Output Buffer DQ,DQS / MR1 bit A12	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]
Burst length	n.a.
Active banks	Refresh command every t_{RFC}=t_{RFC}min
Idle banks	none
Precharge Power Down Mode / Mode Register Bit	n.a.

Table 11 IDD Measurement Conditions for IDD6 and IDD6ET

Current	IDD6	IDD6ET
Name	Self-Refresh Current Normal Temperature Range TCASE = 0 .. 85°C	Self-Refresh Current Extended Temperature Range a TCASE = 0 .. 95°C
Measurement Condition		
Temperature	TCASE = 85°C	TCASE = 95°C
Auto Self Refresh(ASR) / MR2 Bit A6	Disabled / "0"	Disabled / "0"
Self Refresh Temperature Range (SRT) / MR2 Bit A7	Disabled / "0"	Enabled / "1"
CKE	LOW	LOW
External Clock	OFF; CK and $\overline{CK}$ at LOW	OFF; CK and $\overline{CK}$ at LOW
t_{CK}	n.a.	n.a.
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	FLOATING	FLOATING
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	FLOATING	FLOATING
Row, Column Addresses	FLOATING	FLOATING
Bank Addresses	FLOATING	FLOATING
Data I/O	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all during self-refresh actions	all during self-refresh actions
Idle banks	all btw. Self-Refresh actions	all btw. Self-Refresh actions
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.

a. this is applicable only for devices which support the extended temperature - refer to the supplier datasheet for availability and values.

10.9 Input/Output capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input capacitance, CK and $\overline{CK}$	CCK	TBD	1.60	TBD	1.60	TBD	TBD	TBD	TBD	pF	1,2,7
Input capacitance delta, CK and $\overline{CK}$	CDCK	0	0.2	0	0.2	TBD	TBD	TBD	TBD	pF	1,2,6
Input capacitance, all other input-only pins	CI	TBD	1.5	TBD	1.5	TBD	TBD	TBD	TBD	pF	1,2
Input capacitance delta, all control input-only pins	CDI_CTRL	-0.5	0.3	-0.5	0.3	TBD	TBD	TBD	TBD	pF	1,2,4
Input capacitance delta, all CA and CMD pins	CDI_MA_CMD	-0.5	0.5	-0.5	0.5	TBD	TBD	TBD	TBD	pF	1,2,5
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	1.5	3.0	1.5	3.0	1.5	2.5	1.5	TBD	pF	1,2
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	-0.5	0.3	-0.5	0.3	TBD	TBD	TBD	TBD	pF	1,2,3

Note :
1. Pin capacitance specs at 100MHz.
2. Non-stacked (monolith) DDR3 spec. Stacked devices pin parasites are TBD.
3. CDIO=CIO(DQ)-CIO(DQS), Max delta CIO between DQS and $\overline{DQS}$ noting that this value includes the effect of coupling as well as ODT-on and ODT-off.
4. CDI_CTRL= CI(CTRL)-CCK, CTRL pins defined as ODT, CS and CKE, MA pins defined as A0-A15, BA0-BA3 and CMD pins are defined as RAS, CAS and WE
5. CDI_MA_CMD = CI(MA_CMD)-CCK, CTRL pins defined as ODT, CS and CKE, MA pins defined as A0-A15, BA0-BA3 and CMD pins are defined as RAS, CAS and WE
6. Absolute value of CCK-$\overline{CCK}$
7. The minimum CCK will be same with minimum CI

11.0 Electrical Characteristics and AC timing

(0 °C<T_{CASE} ≤95 °C, V_{DDQ} = 1.5V ± 0.075V; V_{DD} = 1.5V ± 0.075V)

11.1 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
All Bank Refresh to active/refresh cmd time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

11.2 DDR3 SDRAM standard speed bins and tRCD, tRP and tRC for corresponding bin

Speed	DDR3-800		DDR3-1066			DDR3-1333		DDR3-1600		Units	Note
Bin (CL - tRCD - tRP)	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	8-8-8	9-9-9	9-9-9	10-10-10		
Parameter	min	min	min	min	min	min	min	min	min		
CL	5	6	6	7	8	8	9	9	10	tCK	
tRCD	12.5	15	11.25	13.13	15	12	13.5	11.25	12.5	ns	
tRP	12.5	15	11.25	13.13	15	12	13.5	11.25	12.5	ns	
tRAS	37.5	37.5	37.5	37.5	37.5	36	36	TBD	TBD	ns	
tRC	50	52.5	48.75	50.63	52.5	48	49.5	TBD	TBD	ns	
tRRD [1KB]	10	10	7.5	7.5	7.5	6.0	6.0	6.0	6.0	ns	
tRRD [2KB]	10	10	10	10	10	7.5	7.5	7.5	7.5	ns	
tFAW [1KB]	40	40	37.5	37.5	37.5	30	30	30	30	ns	
tFAW [2KB]	50	50	50	50	50	45	45	40	40	ns	

DDR3-800 Speed Bins

Speed		DDR3-800D		DDR3-800E		Units	Note
CL-nRCD-nRP		5 - 5 - 5		6 - 6 - 6			
Parameter	Symbol	min	max	min	max		
Internal read command to first data	t_{AA}	12.5	20	15	20	ns	
ACT to internal read or write delay time	t_{RCD}	12.5	-	15	-	ns	
PRE command period	t_{RP}	12.5	-	15	-	ns	
ACT to ACT or REF command period	t_{RC}	50	-	52.5	-	ns	
ACT to PRE command period	t_{RAS}	37.5	9*tREFI	37.5	9*tREFI	ns	9)
CL = 5 / CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		ns	1)2)3)4)
CL = 6 / CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1)2)3)
Supported CL Settings		5,6		6		n_{CK}	
Supported CWL Settings		5		5		n_{CK}	

DDR3-1066 Speed Bins

Speed			DDR3-1066E		DDR3-1066F		DDR3-1066G		Units	Note
CL-nRCD-nRP			6 - 6 - 6		7 - 7 - 7		8 - 8 - 8			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	11.25	20	13.125	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	11.25	-	13.125	-	15	-	ns	
PRE command period		t_{RP}	11.25	-	13.125	-	15	-	ns	
ACT to ACT or REF command period		t_{RC}	48.75	-	50.625	-	52.5	-	ns	
ACT to PRE command period		t_{RAS}	37.5	9*tREFI	37.5	9*tREFI	37.5	9*tREFI	ns	9)
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	Reserved		Reserved		ns	1)2)3)6)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	1.875	<2.5	Reserved		ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1)2)3)
Supported CL Settings			5,6,7,8		6,7,8		6,8		n_{CK}	
Supported CWL Settings			5,6		5,6		5,6		n_{CK}	

DDR3-1333 Speed Bins

Speed			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Units	Note
CL-nRCD-nRP			7 - 7 - 7		8 - 8 - 8		9 -9 - 9		10 - 10 - 10			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	10.5	20	12	20	13.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	10.5	-	12	-	13.5	-	15	-	ns	
PRE command period		t_{RP}	10.5	-	12	-	13.5	-	15	-	ns	
ACT to ACT or REF command period		t_{RC}	46.5	-	48	-	49.5	-	51	-	ns	
ACT to PRE command period		t_{RAS}	36	9*tREFI	36	9*tREFI	36	9*tREFI	36	9*tREFI	ns	9)
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	Reserved		Reserved		ns	1)2)3)4)7)
	CWL = 6,7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)3)7)
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	Reserved		Reserved		Reserved		ns	1)2)3)4)7)
	CWL = 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	1.875	<2.5	Reserved		Reserved		ns	1)2)3)4)7)
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	1.875	<2.5	1.875	<2.5	1.875	<2.5	ns	1)2)3)7)
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1)2)3)4)
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4)
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1)2)3)4)
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4)
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1)2)3)
			(Optional)		(Optional)		(Optional)		(Optional)		ns	5)
Supported CL Settings			5,6,7,8,9		5,6,7,8,9		6,8,9		6,8,10		n_{CK}	
Supported CWL Settings			5,6,7		5,6,7		5,6,7		5,6,7		n_{CK}	

11.3 Input clock Jitter

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		min	max	min	max	min	max	min	max	
Average clock period	tCK(avg)	2500	3333	1875	3333	1500	3333	1250	3333	ps
Clock period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge

$$\left(\sum_{j=1}^{N} tCKj \right) \Big/ N \qquad N=200$$

tCK(abs) is the absolute clock period, as measured from one rising edge to the next consecutive rising edge

Parameter	Symbol	DDR3-800		DDR3-800		DDR3-800		DDR3-800		Units
		min	max	min	max	min	max	min	max	
Clock period jitter	tJIT(per)	-100	100	-90	90	TBD	TBD	TBD	TBD	ps
Clock period jitter during DLL locking period	tJIT(per,lck)	-90	90	-80	80	TBD	TBD	TBD	TBD	ps
Cycle to cycle clock period jitter	tJIT(cc)	200		180		TBD	TBD	TBD	TBD	ps
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	180		160		TBD	TBD	TBD	TBD	ps
Cumulative error across 2cycles	tERR(2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative error across 3cycles	tERR(3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative error across 4cycles	tERR(4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative error across 5cycles	tERR(5per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative error across 6,7,8,9,10 cycles	tERR(6~10per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
Cumulative error across 11~50 cycles	tERR(11~50per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	TBD	TBD	TBD	TBD	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	TBD	TBD	TBD	TBD	tCK(avg)
Duty cycle jitter	tJIT(duty)	-100	100	-75	75	TBD	TBD	TBD	TBD	ps

Note: The jitter specified is a random jitter meeting a Gaussian distribution

Add note for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses:

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses:

$$\left(\sum_{j=1}^{N} tCHj \right) \Big/ N \times tCK(avg) \qquad N=200$$

$$\left(\sum_{j=1}^{N} tCLj \right) \Big/ N \times tCK(avg) \qquad N=200$$

Add note for tJIT(duty)

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH form tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg)

tJIT(duty) = min/max of {tJIT(CH), tJIT(CL)}, where:

tJIT(CH) = {tCHi-tCH(avg) where i=1 to 200}, tJIT(CL) = {tCLi-tCL(avg) where i=1 to 200},

Add note for tJIT(per), tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). tJIT(per) = min/max of {tCKi-tCK(avg) where i=1 to 200}
tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing

Add note for tJIT(cc), tJIT(cc,lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of {tCKi+1-tCKi}
tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing

Add note for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). This definition is TBD

11.4 Timing parameters for DDR3-800 and DDR3-1066

Timing Parameters by Speed Bin

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	8	-	8	-	ns	6
Average Clock Period	$t_{CK(avg)}$	See Speed Bins Table						ps	f
Clock Period	$t_{CK(abs)}$	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Clock Period Jitter	$tJIT_{(per)}$	-100	100	-90	90	-80	80	ps	
Clock Period Jitter during DLL locking period	$tJIT_{(per, lck)}$	-90	90	-80	80	-70	70	ps	
Cycle to Cycle Period Jitter	$tJIT_{(cc)}$	200		180		160		ps	
Cycle to Cycle Period Jitter during DLL locking period	$tJIT_{(cc, lck)}$	180		160		140		ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across n = 6, 7, 8, 9, 10 cycles	$t_{ERR(6-10per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across n = 11, 12, ... 49, 50 cycles	$t_{ERR(11-50per)}$	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	f
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	f
Duty Cycle Jitter	$t_{JIT(duty)}$	-100	100	-75	75	-60	60	ps	22
Data Timing									
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	200	-	150	-	125	ps	12,13
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.36	-	0.36	-	0.36	-	$t_{CK(avg)}$	12,13
DQ low-impedance time from CK, $\overline{CK}$	$t_{LZ(DQ)}$	-800	400	-600	300	-500	250	ps	12,13,14
DQ high-impedance time from CK, $\overline{CK}$	$t_{HZ(DQ)}$	-	400	-	300	-	250	ps	12,13,14
Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	$t_{DS(base)}$	75	-	25	-	TBD	-	ps	d, 17
Data hold time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	$t_{DH(base)}$	150	-	100	-	TBD	-	ps	d, 17
DQ and DM input pulse width for each input	t_{DIPW}	0.35	-	0.35	-	0.35	-	$t_{CK(avg)}$	
Data Strobe Timing									
DQS, $\overline{DQS}$ READ Preamble	t_{RPRE}	0.9	-	0.9	-	0.9	-	t_{CK}	1, 19
DQS, $\overline{DQS}$ differential READ Postamble	t_{RPST}	0.3	NOTE1	0.3	NOTE1	0.3	NOTE1	t_{CK}	11,12,13
DQS, $\overline{DQS}$ output high time	t_{QSH}	0.38	-	0.38	-	0.38	-	$t_{CK(avg)}$	12,13
DQS, $\overline{DQS}$ output low time	t_{QSL}	0.38	-	0.38	-	0.38	-	$t_{CK(avg)}$	12,13
DQS, $\overline{DQS}$ WRITE Preamble	t_{WPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	1
DQS, $\overline{DQS}$ WRITE Postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	1
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-350	350	-265	265	-225	225	ps	12,13
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	$t_{LZ(DQS)}$	-800	400	-600	300	-500	250	ps	12,13,14
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	$t_{HZ(DQS)}$	-	400	-	300	-	250	ps	12,13,14
DQS, $\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS, $\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	t_{DQSS}	-0.25	0.25	-0.25	0.25	-0.25	0.25	$t_{CK(avg)}$	c
DQS,$\overline{DQS}$ faling edge setup time to CK, $\overline{CK}$ rising edge	t_{DSS}	0.2	-	0.2	-	0.2	-	$t_{CK(avg)}$	c
DQS,$\overline{DQS}$ faling edge hold time to CK, $\overline{CK}$ rising edge	t_{DSH}	0.2	-	0.2	-	0.2	-	$t_{CK(avg)}$	c

Timing Parameters by Speed Bin (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
DLL locking time	t_{DLLK}	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	t_{RTP}	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	t_{WTR}	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,7.5ns)	-		e,18
WRITE recovery time	t_{WR}	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	t_{MRD}	4	-	4	-	4	-	$t_{CK(avg)}$	
Mode Register Set command update delay	t_{MOD}	max ($12t_{CK}$,15ns)	-	max ($12t_{CK}$,15ns)	-	max ($12t_{CK}$,15ns)	-		
ACTIVE to PRECHARGE command period	t_{RAS}	37.5	70,000	37.5	70,000	36	70,000	ns	e
ACTIVE to ACTIVE command period for 1KB page size	t_{RRD}	max ($4t_{CK}$,10ns)	-	max ($4t_{CK}$,7.5ns)	-	max ($4t_{CK}$,6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	t_{RRD}	max ($4t_{CK}$,10ns)	-	max ($4t_{CK}$,10ns)	-	max ($4t_{CK}$,7.5ns)	-		e
Four activate window for 1KB page size	t_{FAW}	40	-	37.5	-	30	-	ns	e
Four activate window for 2KB page size	t_{FAW}	50	-	50	-	45	-	ns	e
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IS(base)}$	200	-	125	-	TBD	-	ps	b,16
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IH(base)}$	275	-	200	-	TBD	-	ps	b,16
Control & Address input pulse width for each input	t_{IPW}	0.6	-	0.6	-	0.6	-	$t_{CK(avg)}$	
Multi Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	1	-	nCK	23
Refresh Timing									
512Mb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	t_{RFC}	90	-	90	-	90	-	ns	
1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	t_{RFC}	110	-	110	-	110	-	ns	
2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	t_{RFC}	160	-	160	-	160	-	ns	
4Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	t_{RFC}	300	-	300	-	300	-	ns	
8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	t_{RFC}	350	-	350	-	350	-	ns	
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	t_{REFI}	7.8		7.8		7.8		us	
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	t_{REFI}	3.9		3.9		3.9		us	
Calibration Timing									
Power-up and RESET calibration time	$t_{ZQinitI}$	512	-	512	-	512	-	t_{CK}	
Normal operation Full calibration time	t_{ZQoper}	256	-	256	-	256	-	t_{CK}	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	64	-	t_{CK}	
Reset Timing									
Exit Reset from CKE HIGH to a valid command	t_{XPR}	max($5t_{CK}$, t_{RFC} + 10ns)	-	max($5t_{CK}$, t_{RFC} + 10ns)	-	max($5t_{CK}$, t_{RFC} + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	max($5t_{CK}$,t_{RFC} + 10ns)	-	max($5t_{CK}$,t_{RFC} + 10ns)	-	max($5t_{CK}$,t_{RFC} + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{CK}	
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) + $1t_{CK}$	-	t_{CKE}(min) + $1t_{CK}$	-	t_{CKE}(min) + $1t_{CK}$	-		
Valid Clock Requirement after Self Refresh Entry (SRE)	t_{CKSRE}	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX)	t_{CKSRX}	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-	max($5t_{CK}$,10ns)	-		

Timing Parameters by Speed Bin (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Percharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max ($3t_{CK}$,7.5ns)	-	max ($3t_{CK}$,7.5ns)	-	max ($3t_{CK}$,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	max ($10t_{CK}$,24ns)	-	max ($10t_{CK}$,24ns)	-	max ($10t_{CK}$,24ns)	-		2
CKE minimum pulse width	t_{CKE}	max ($3t_{CK}$,7.5ns)	-	max ($3t_{CK}$,5.625ns)	-	max ($3t_{CK}$,5.625ns)	-		
Command pass disable delay	t_{CPDED}	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	$9*t_{REFI}$	t_{CKE}(min)	$9*t_{REFI}$	t_{CKE}(min)	$9*t_{REFI}$	t_{CK}	15
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	t_{PRPDEN}	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN}	WL + 4 +(t_{WR}/t_{CK})	-	WL + 4 +(t_{WR}/t_{CK})	-	WL + 4 +(t_{WR}/t_{CK})	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	t_{WRPDEN}	WL + 2 +(t_{WR}/t_{CK})	-	WL + 2 +(t_{WR}/t_{CK})	-	WL + 2 +(t_{WR}/t_{CK})	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	$t_{WRAPDEN}$	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-	t_{CK}	
ODT Timing									
ODT high time without write command or with wirte command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	t_{AONPD}	1	9	1	9	1	9	ns	
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	t_{AOFPD}	1	9	1	9	1	9	ns	
ODT turn-on	t_{AON}	-400	400	-300	30	-250	250	ps	7,12
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	8,12
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	12
Write Leveling Timing									
First DQS pulse rising edge after tDQSS margining mode is programmed	t_{WLMRD}	40	-	40	-	40	-	t_{CK}	3
DQS/DQS delay after tDQS margining mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	t_{CK}	3
Setup time for tDQSS latch	t_{WLS}	0.15	-	0.15	-	0.15	-	$t_{CK(avg)}$	
Hold time of tDQSS latch	t_{WLH}	0.15	-	0.15	-	0.15	-	$t_{CK(avg)}$	
Write leveling output delay	t_{WLO}	0	9	0	9	0	9	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	ns	
Write Leveling System specific design guidelines (reference)									
Write leveling window: System Clock and strobe signal routing to be matched within TBD	t_{WLW}	-0.4	0.4	-0.4	0.4	-0.4	0.4	t_{CK}	
Write leveling repetetition time	t_{WLR}	16	-	16	-	16	-	t_{CK}	3

Jitter Notes

Specific Note a
Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.

Specific Note b
These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
ex) Input setup/hold parameters specifying clock to input relationship; such as, tIS(base).tIH(base),etc.

Specific Note c
These parameters are measured from a data strobe signal (DQS(L/U)/$\overline{DQS(L/U)}$) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
ex) the parameters specifying clock to strobe relationship; such as tDQSS, tDSS, tDSH, etc.

Specific Note d
These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U)/$\overline{DQS(L/U)}$) crossing.
ex) Data input setup/hold parameters specifying strobe to data input relationship; such as,tDS(base), tDH(base), etc.

Specific Note e
For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
ex) Most parameters specifying DRAM core timings; such as tRCD, tRP, tRC, tRAS, tRRD, tFAW, tWR, tWTR, tRTP, etc.

Specific Note f
These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Min and Max SPEC values

Parameter	Symbol	Min	Max	Units
Absolute clock period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min X tCK(avg),min + tJIT(duty),min	tCH(avg),max X tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min X tCK(avg),min + tJIT(duty),min	tCL(avg),max X tCK(avg),max + tJIT(duty),max	ps

Example: For DDR3-800, tCH(abs),min=(0.48X2500ps)-100ps=1100ps, if tCH(avg),min=0.48tCK(avg) and tJIT(duty),min=-100ps

Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.

2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

3. The max values are system dependent.

4. WR as programmed in mode register

5. Value must be rounded-up to next higher integer value

6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

7. For definition of RTT turn-on time tAON see "Device Operation"

8. For definition of RTT turn-off time tAOF see "Device Operation".

9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

10. WR in clock cycles as programmed in MR0

11. The maximum postamble is bound by tHZDQS(max)

12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD

13. Value is only valid for RON34

14. Single ended signal parameter. Refer to chapter <TBD> for definition and measurement method.

15. tREFI depends on TOPER

16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate, Note for DQ and DM signals, VREF(DC) = VrefDQ(DC). FOr input only pins except RESET, VRef(DC)=VRefCA(DC).
See "Address/ Command Setup, Hold and Derating" on page 46.

17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, VREF(DC)= VRefDQ(DC). For input only pins except RESET, VRef(DC)=VRefCA(DC).
See "Data Setup, Hold and Slew Rate Derating" on page 47.

18. Start of internal write transaction is definited as follows ;
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL

19. The maximum preamble is bound by tLZDQS(max)

20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

21. Altough CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".

22. tJIT(duty) = +/- {0.07 * tCK(avg) - [(p.5 - (min (tCH(avg), tCL(avg))) * tCK(avg)]}.
For example, if tCH/tCL was 0.48/0.52, tJIT(duty) would calculated out to +/- 125ps for DDR3-800. The tCH(abg) and tCL(avg) values listed must not be exceeded.

Address / Command Setup, Hold and Derating:

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 4) to the ΔtIS and ΔtIH derating value (see Table 5) respectively.
Example: tIS (total setup time) = tIS(base) + ΔtIS Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as
the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value (see Figure 1). If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 3).
Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value (see Figure 2). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 4).
For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see Table 6).
Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).
For slew rates in between the values listed in Table 5, the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization.

ADD/CMD Setup and Hold Base-Values for 1V/ns

[ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	reference
tIS(base)	200	125	TBD	TBD	$V_{IH/L(ac)}$
tIH(base)	275	200	TBD	TBD	$V_{IH/L(dc)}$

Note : AC/DC referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate

Derating values DDR3-800/1066 tIS/tIH-ac/dc based

ΔtIS, ΔtIH Derating [ps] AC/DC based[a]																
		CLK,$\overline{CLK}$ Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	74
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	20	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	13	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	6	10
	0.4	-62	-60	-62	-60	-60	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Required time t_{VAC} above VIH(ac) {blow VIL(ac)} for valid transition

Slew Rate[V/ns]	t_{VAC}[ps]	
	min	max
>2.0	75	-
2.0	57	-
1.5	50	-
1.0	38	-
0.9	34	-
0.8	29	-
0.7	22	-
0.6	13	-
0.5	0	-
< 0.5	0	-

Note :Clock and Strobe are drawn on a different time scale.

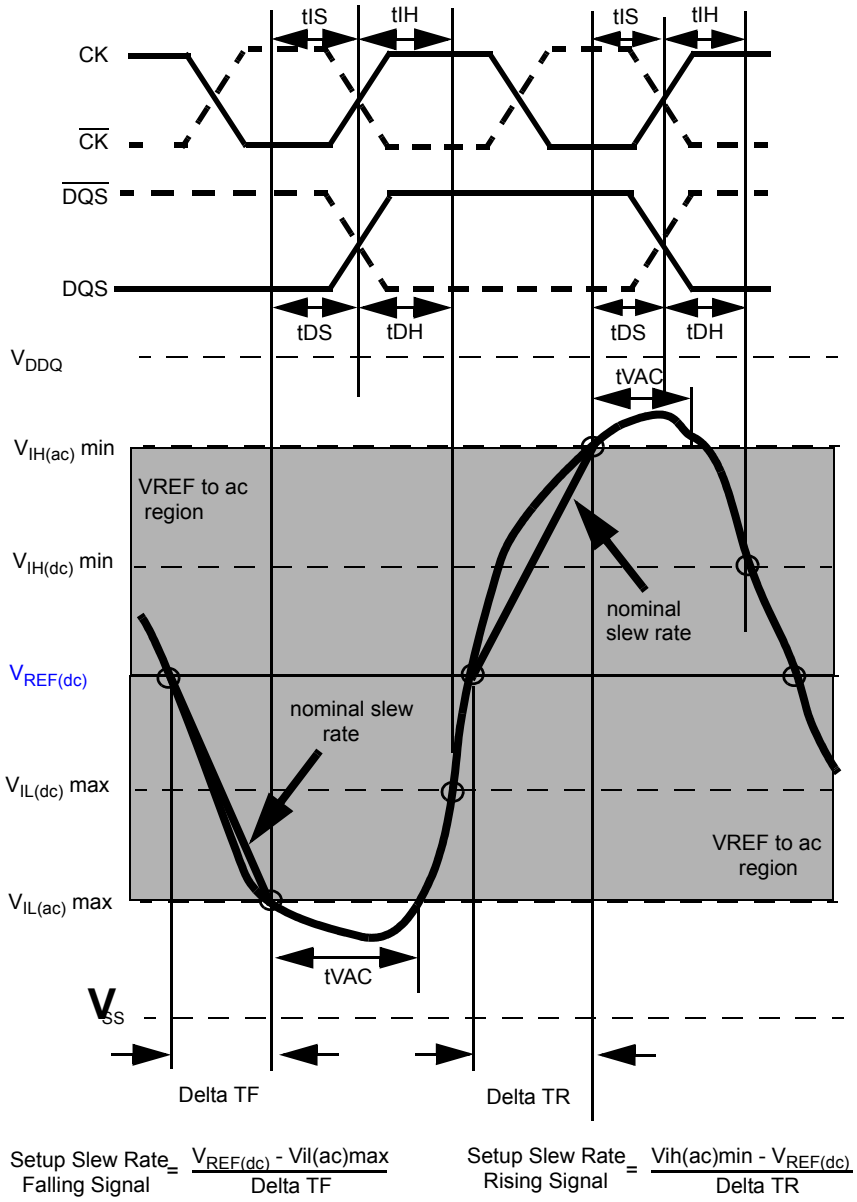


Figure - Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

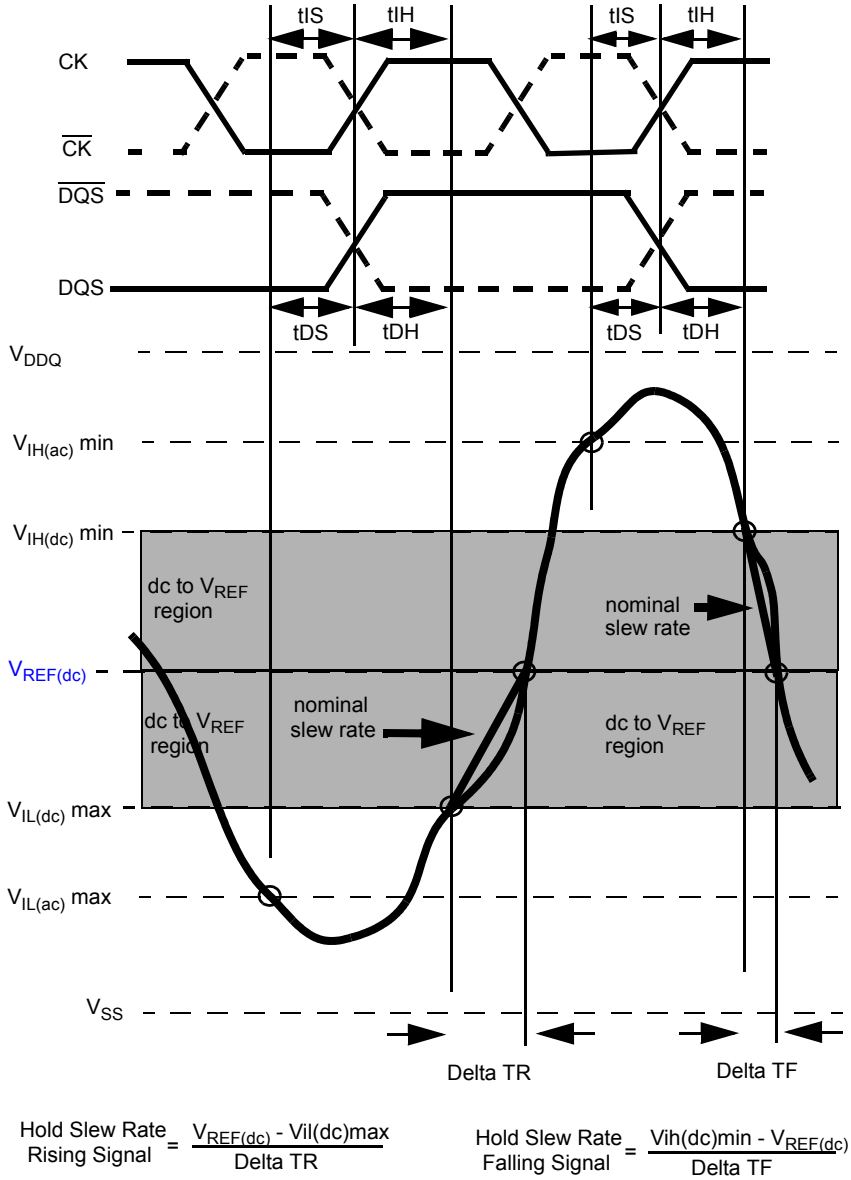


Figure - Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

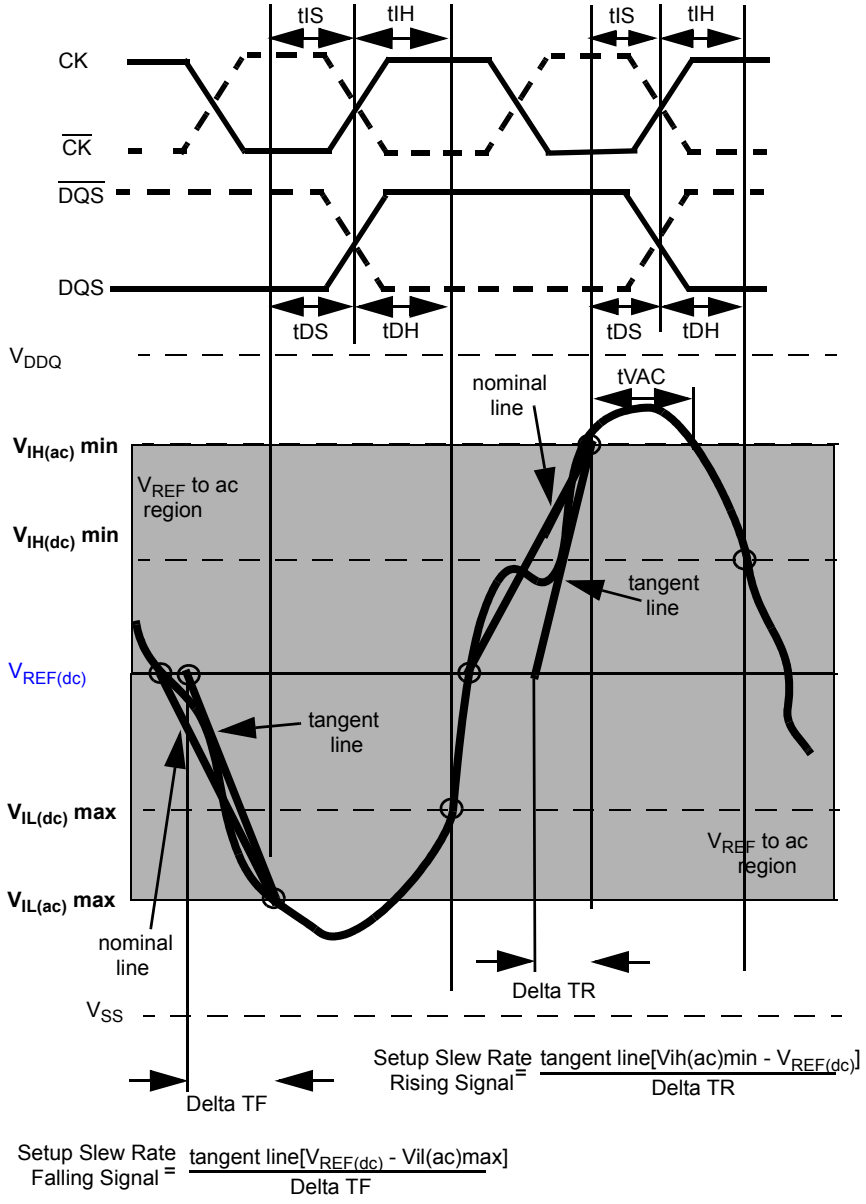


Figure - Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock)

Note :Clock and Strobe are drawn on a different time scale.

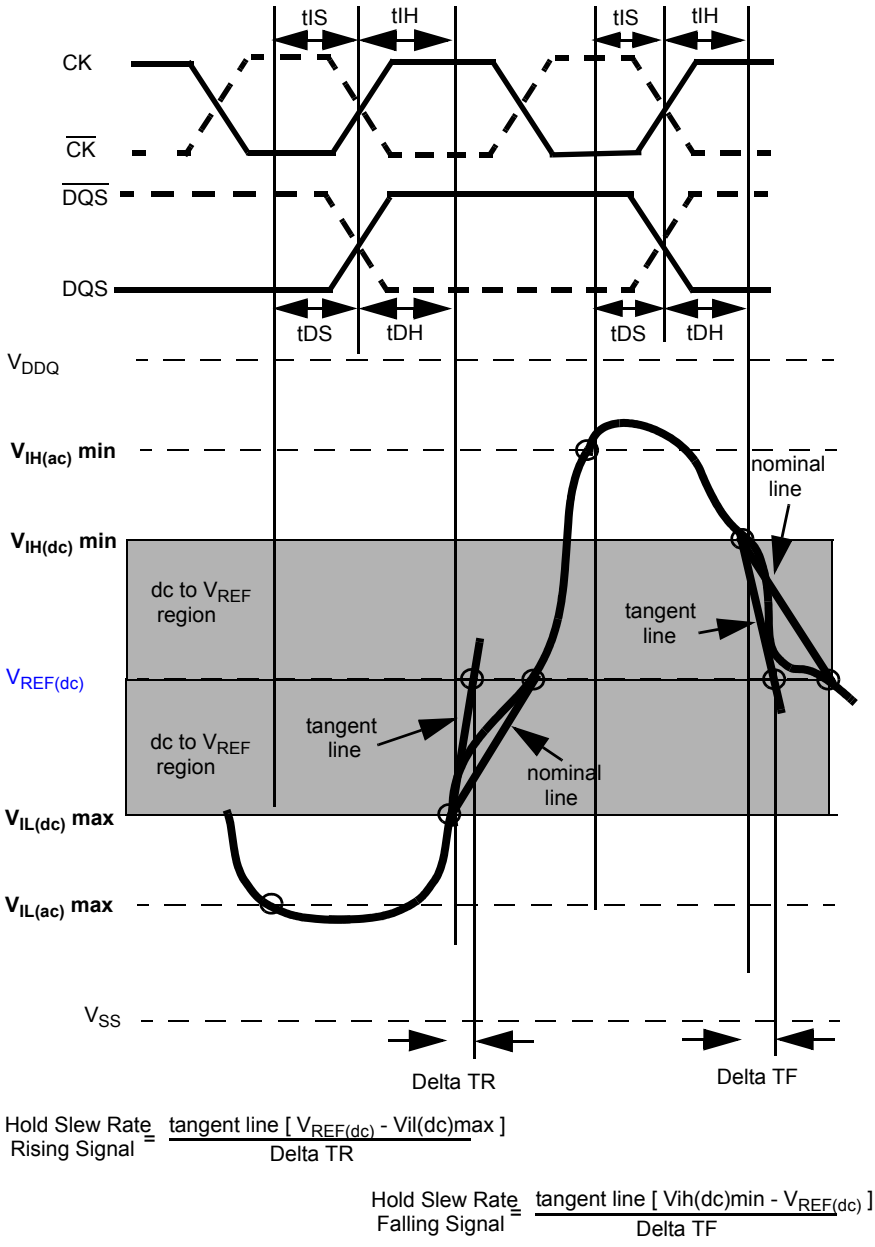


Figure - Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)

Data Setup, Hold and Slew Rate Derating:

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 1) to the Δ tDS and ΔtDH (see Table 2) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.
Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max (see Figure 1). If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere
between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 3).
Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc) (see Figure 2). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value (see Figure 4).

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC (see Table 3).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).
For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization

[Table 53] Data Setup and Hold Base-Value

[ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	reference
tDS(base)	75	25	TBD	TBD	$V_{IH/L(ac)}$
tDH(base)	150	100	TBD	TBD	$V_{IH/L(dc)}$

Note : AC/DC referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

[Table 54] Derating values DDR3-800/1066 tIS/tIH-ac/dc based

ΔtDS, ΔtDH Derating [ps] AC/DC based[a]																
		DQS,DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	45	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	6	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

Note : a. Cell contents shaded in red are defined as 'not supported'.

[Table 55] Required time t_{VAC} above VIH(ac) {blow VIL(ac)} for valid transition

Slew Rate[V/ns]	t_{VAC}[ps]	
	min	max
>2.0	75	-
2.0	57	-
1.5	50	-
1.0	38	-
0.9	34	-
0.8	29	-
0.7	22	-
0.6	13	-
0.5	0	-
<0.5	0	-

Note :Clock and Strobe are drawn on a different time scale.

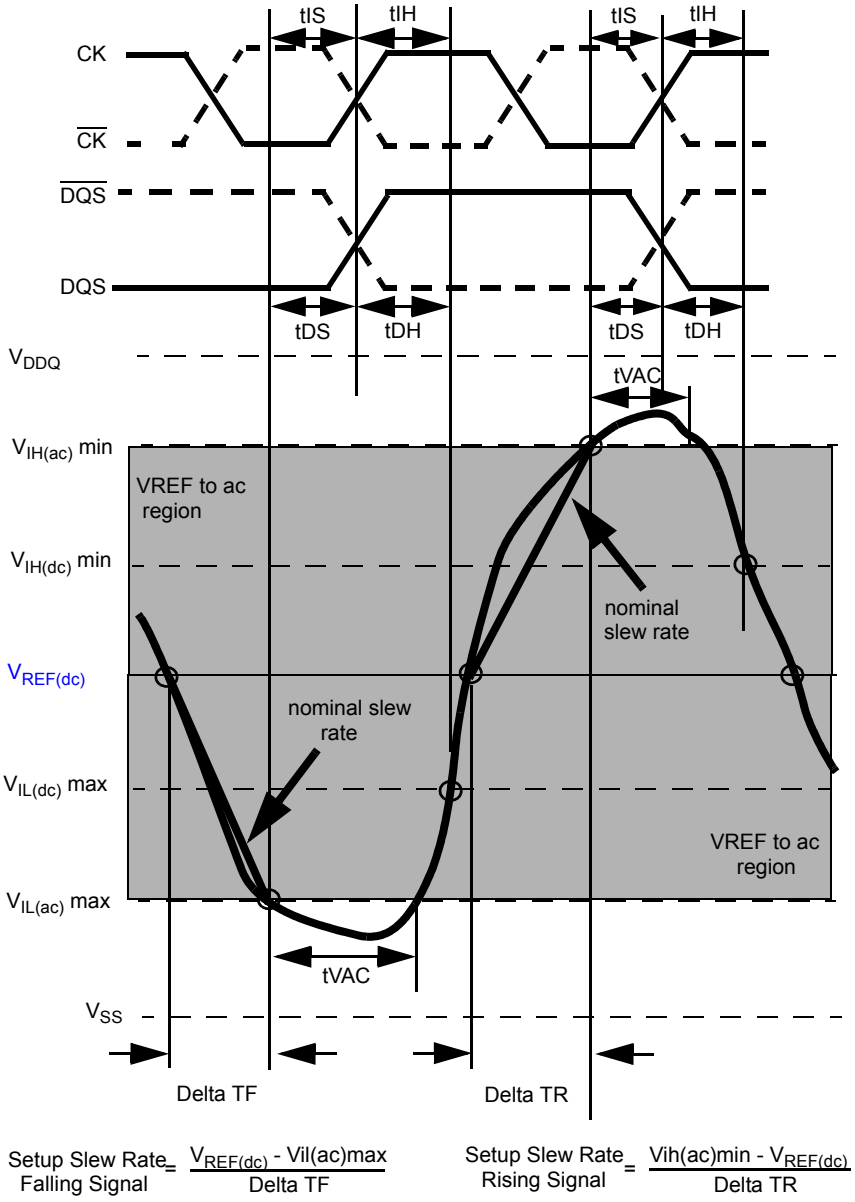


Figure - Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

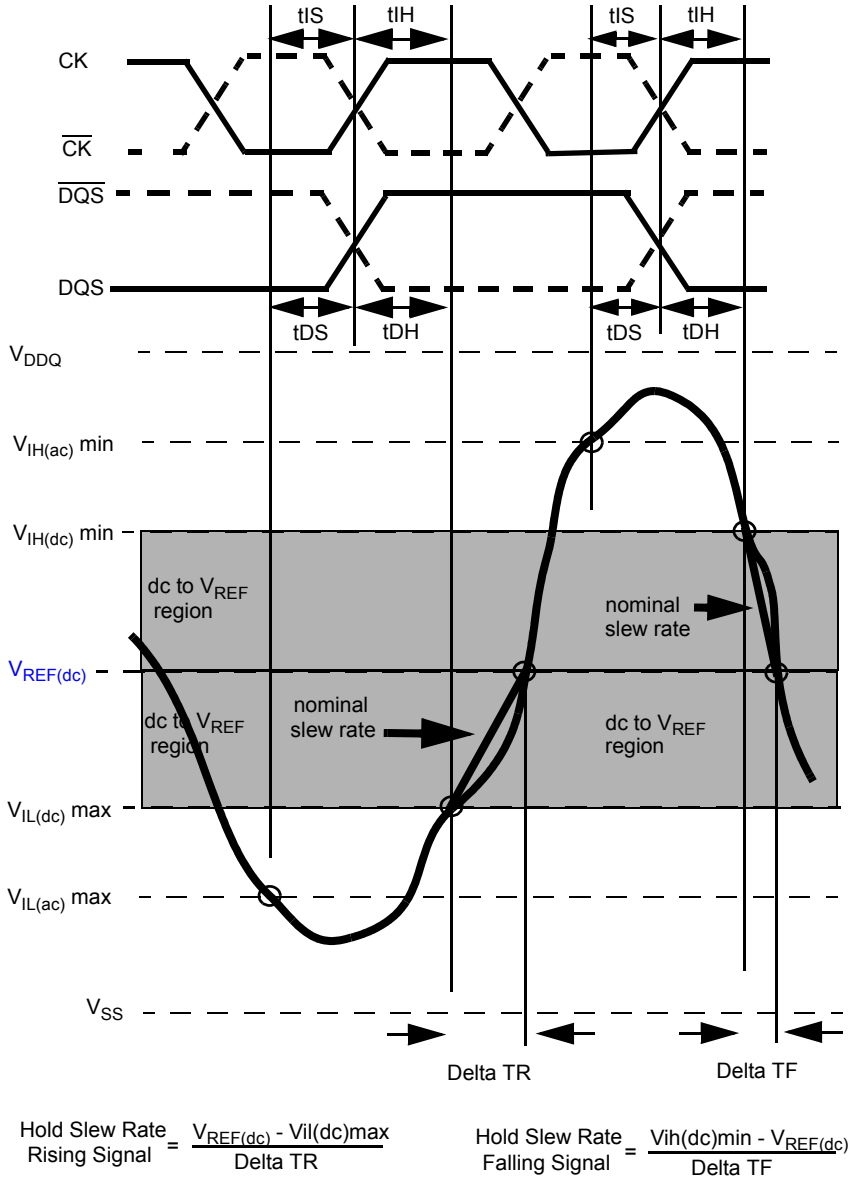


Figure - Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

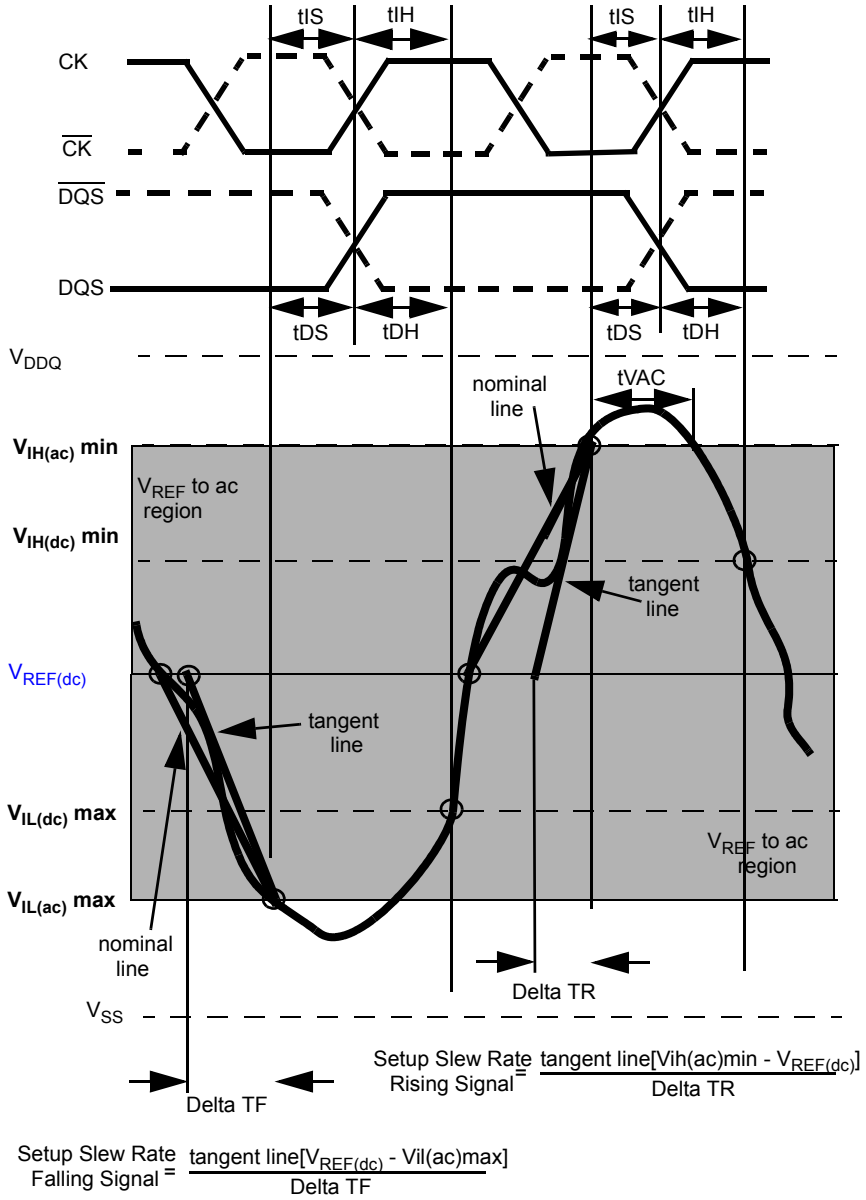


Figure - Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock)

Note :Clock and Strobe are drawn on a different time scale.

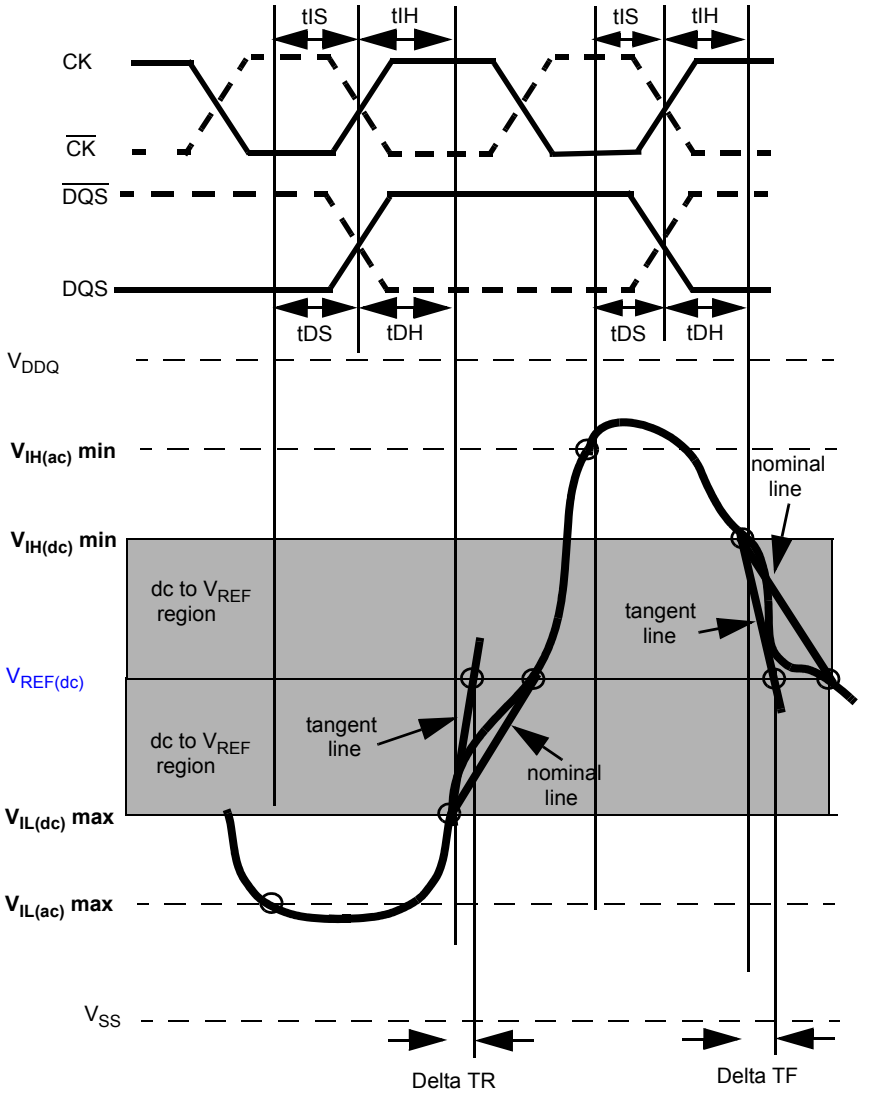
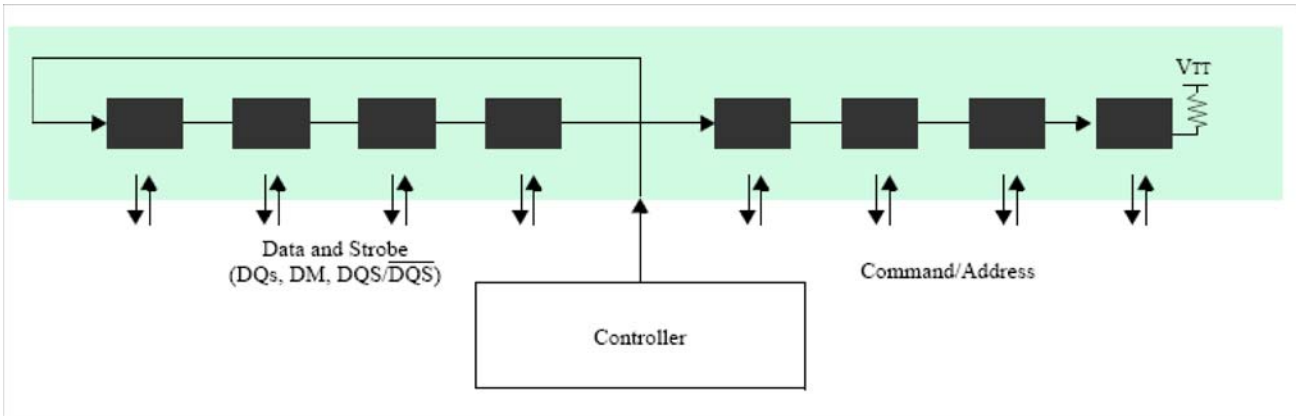


Figure - Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)

Signal Groups

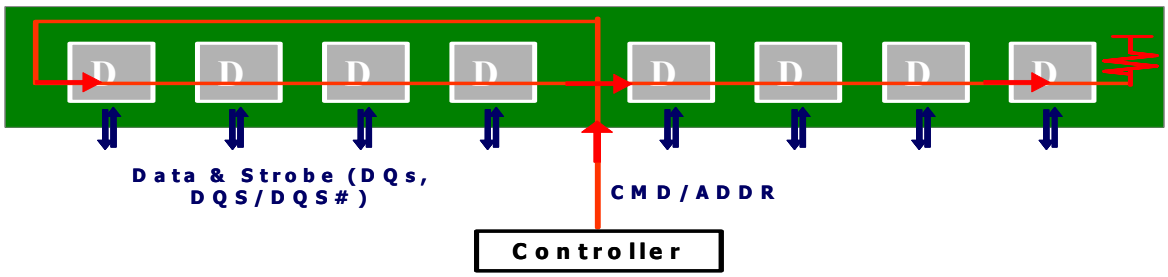
This specification categorizes DDR3 SDRAM timing-critical signals into four groups. The following table summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. They sweep from the left side of the module to the right.



Timing-Critical Signals

Signal Group	Signals In Group	Raw Card Version
Clock	CK0, CK0	A, C, D
	CK0, CK0, CK1, CK1	B, E, F
Data	DQ, DM, DQS, DQS	A, B, C, D, E, F
Control	S0, S1, ODT0, ODT1, CKE0, CKE1	B, E, F
	S0, ODT0, CKE0	A, C, D
Address/Command	ADD, CMD	A, B, C, D, E, F

12.0 Write Leveling



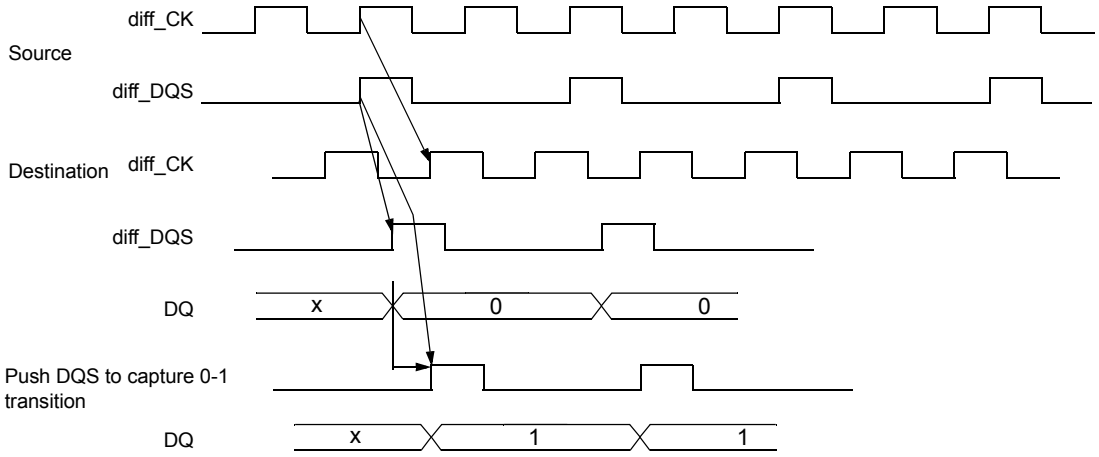
[Figure1] CMD/CTRL/CLK routing topology in DDR3 Module

Description

For better signal integrity, DDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. therefore, the controller should support 'write leveling' in DDR3 SDRAM to compensate the skew

Write leveling is a scheme to adjust DQS to CK relationship by the controller, with a simple feedback provided by the DRAM. The memory controller involved in the leveling must have adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established through this exercise would ensure tDQSS, tDSS and tDSH specification. A conceptual timing of this scheme is shown as below

Write leveling concept



DQS/$\overline{\text{DQS}}$ driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.
One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4,X8 and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (TABLE1). Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via ODT pin not like normal operation (TABLE2)

TABLE1. MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

TABLE2. DRAM termination function in the leveling mode

ODT pin @DRAM	DQS/$\overline{DQS}$ termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

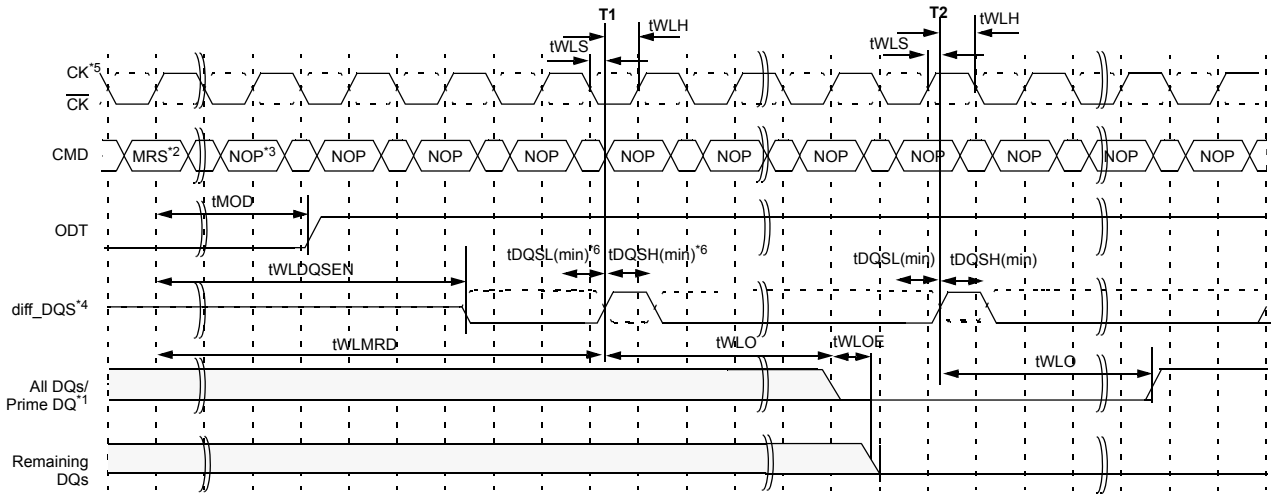
Note: In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

Procedure description

Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed. Since the controller levels one rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.

Controller may drive DQS low and $\overline{DQS}$ high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK driven from controller. tWLMRD(max) timing is controller dependent.
DRAM samples CK status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/$\overline{DQS}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS delay setting and launches the next DQS/$\overline{DQS}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS delay setting and write leveling is achieved for the device. The below figure describes detailed timing diagram for overall procedure and the timing parameters are shown in below figure.

Figure2 : Timing details of Write leveling sequence [DQS is capturing CK low at T1 and CK high at T2]



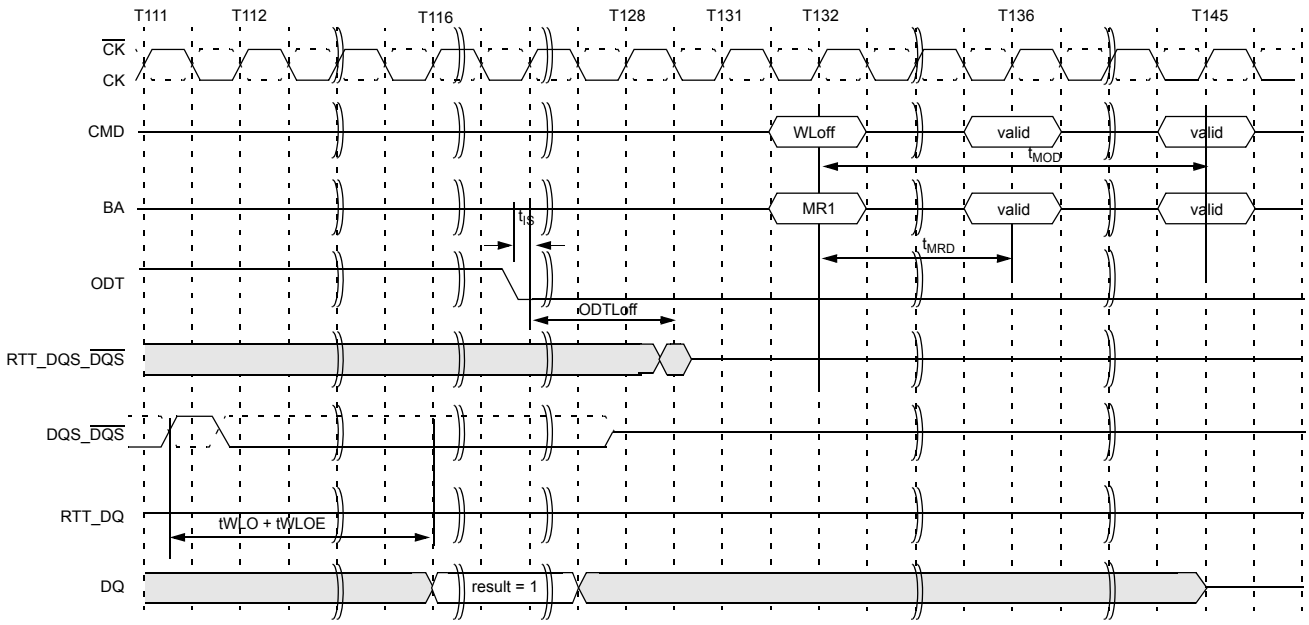
Note *:
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQS must be driven low as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS : Load MR1 to enter write leveling mode
3. NOP : NOP or deselect
4. diff_DQS is the differential data strobe (DQS-$\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line
5. CK/$\overline{CK}$: CK is shown with solid dark line, where as $\overline{CK}$ is drawn with dotted line.
6. DQS needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

Write Leveling Mode Exit

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe (see ~T111) edge stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (T145)
2. Drive ODT pin low (tIS must be satisfied) and keep it low. (see T128)
3. After the RTT is switched off: disable Write Level Mode via MR command (see T132)
4. After tMOD is satisfied (T145), a any valid command may be registered. (MR commands may already be issued after tMRD (T136).

Figure3 : Timing details of Write leveling exit



Related timing parameters

TABLE3. Related timing parameters

Parameter	Description	Target values		units
		Min	Max	
tWLMRD	First DQS pulse rising edge after tDQS margining mode is programmed	40	Note1	tCK
tMOD	Mode register set command update delay	12	Note1	tCK
tWLDQSEN	DQS/$\overline{DQS}$ delay after tDQSS margining mode is programmed	25	Note1	tCK
tWLS	Setup time for tDQSS flop measured from diff_CK zero crossing to rising strobe edge (diff_DQS zero crossing)	0.16	Note1	tCK
tWLH	Hold time of tDQSS flop measured from rising strobe edge (diff_DQS zero crossing) to diff_CK zero crossing edge	0.16	Note1	tCK
tWLO	Write leveling output delay	0	9/7.5[*2]	ns
tWLOE	Write leveling output error	0	2	ns

Note1: The max values are system dependent.
Note2: tWLOmax=9ns for DDR3-800/1066/1333, 7.5ns for DDR3-1600

13.0 MPR and Read Leveling

MPR (Multi Purpose Register)

DDR3 SDRAM has 4 registers (8bits per each register) inside DRAM, called MPR (Multi Purpose Register). MPR can be activated using MR3 and if A2 in MR3 is set 1, the DRAM internal dataflow is changed from DRAM cell array to MPR so User can access (readout only) MPR. each register can be addressed using A1&A0 in MR3.
One of application of MPR is Read leveling (TBD for 3 registers) in order to do system level read timing calibration based on predetermined and standardized pattern. All banks should be precharged before access MPR and DRAM enters MPR mode setting A2 in MR3 to High and select 1st register in MPR setting A1=High and A0=Low which containing predefined 8bit data pattern for read leveling. Now DRAM internal dataflow is set to MPR so after waiting tMOD which is required time to update DRAM internal setting, user can readout the predefined 8bit data pattern (01010101) with issuing read command. the data will come out after normal Read latency. After reading predefined data pattern from MRP, DRAM comes back to normal mode with setting A2 in MR3 to Low

MR3			MPR function	Burst Length	Read address A[2:0]	Burst order and data pattern	Notes
A2	A1	A0					
1	0	0	Predefined pattern for system read calibration	BL8	000	Burst order: 0,1,2,3,4,5,6,7 Pre-defined pattern : 0,1,0,1,0,1,0,1	1,2
				BC4	000	Burst order: 0,1,2,3 Pre-defined pattern : 0,1,0,1	1,2
				BC4	100	Burst order: 4,5,6,7 Pre-defined pattern : 0,1,0,1	1,2
1	0	1	RFU	BL8	000	Burst order: 0,1,2,3,4,5,6,7	1,2
				BC4	000	Burst order: 0,1,2,3	1,2
				BC4	100	Burst order: 4,5,6,7	1,2
1	1	0	RFU	BL8	000	Burst order: 0,1,2,3,4,5,6,7	1,2
				BC4	000	Burst order: 0,1,2,3	1,2
				BC4	100	Burst order: 4,5,6,7	1,2
1	1	1	ODTS	BL8	000	Burst order: 0,1,2,3,4,5,6,7	1,2
				BC4	000	Burst order: 0,1,2,3	1,2
				BC4	100	Burst order: 4,5,6,7	1,2

Note :
1. Burst order bit 0 is assigned to the LSB and burst order bit7 is assigned to the MSB of the selected MPR function.
2. Bank address BA[2:0] and other addresses except A[2:0] and A12/$\overline{BC}$ are Don't Care for Read address.

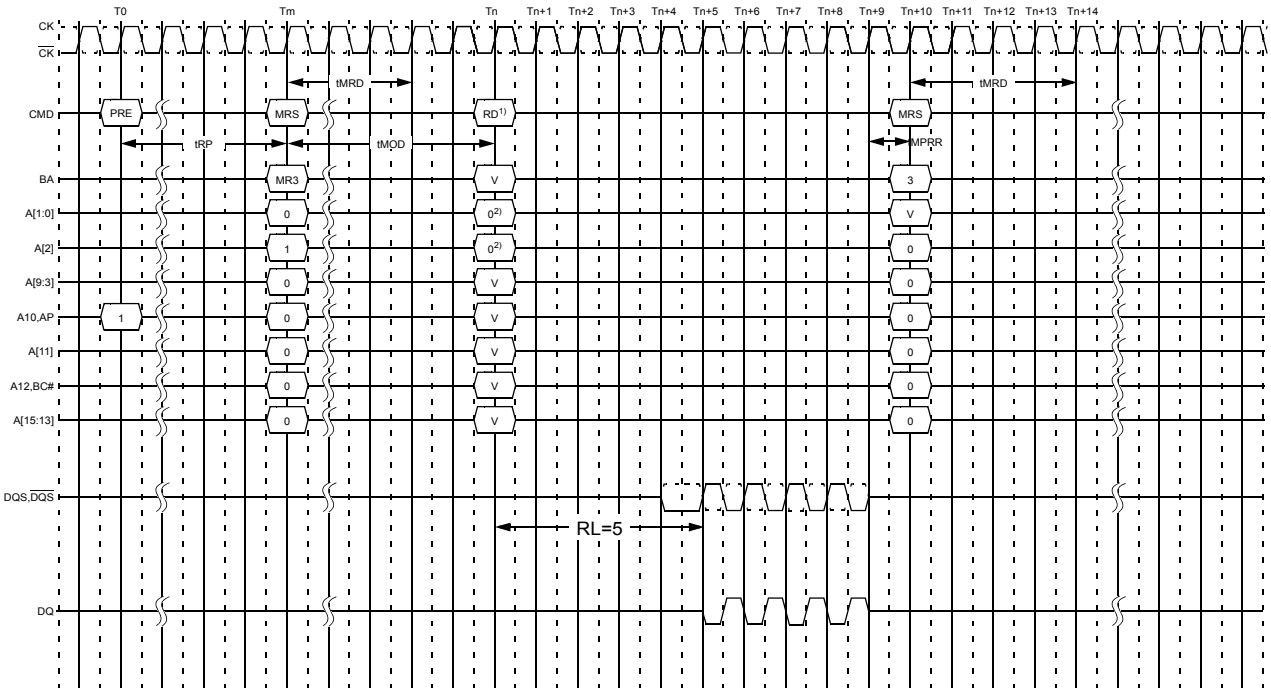
[Data coding]

MR3 Address			MPR function	Burst data coding								Condition	Notes
A2	A1	A0		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
1	0	0	Predefined pattern	0	1	0	1	0	1	0	1	For system read leveling	
1	1	1	ODTS*1	RFU	RFU	RFU	RFU	RFU	RFU	0	0	RFU	1,2
				RFU	RFU	RFU	RFU	RFU	RFU	0	1	Temp < Trip point1 (Tj=~Tc:85C)	1
				RFU	RFU	RFU	RFU	RFU	RFU	1	0	Temp>=Trip point2 (Tj=~Tc:95C)	1
				RFU	RFU	RFU	RFU	RFU	RFU	1	1	TP1(Tj=~Tc:85C)<=Temp<TP2(Tj=~Tc:95C)	1

Note :
1. For MPR output bits defined as RFU, DRAM must output a logical 0.
2. DRAM's supporting the ODTS feature may not output this code

Readout of predefined pattern for system read calibration with BL8

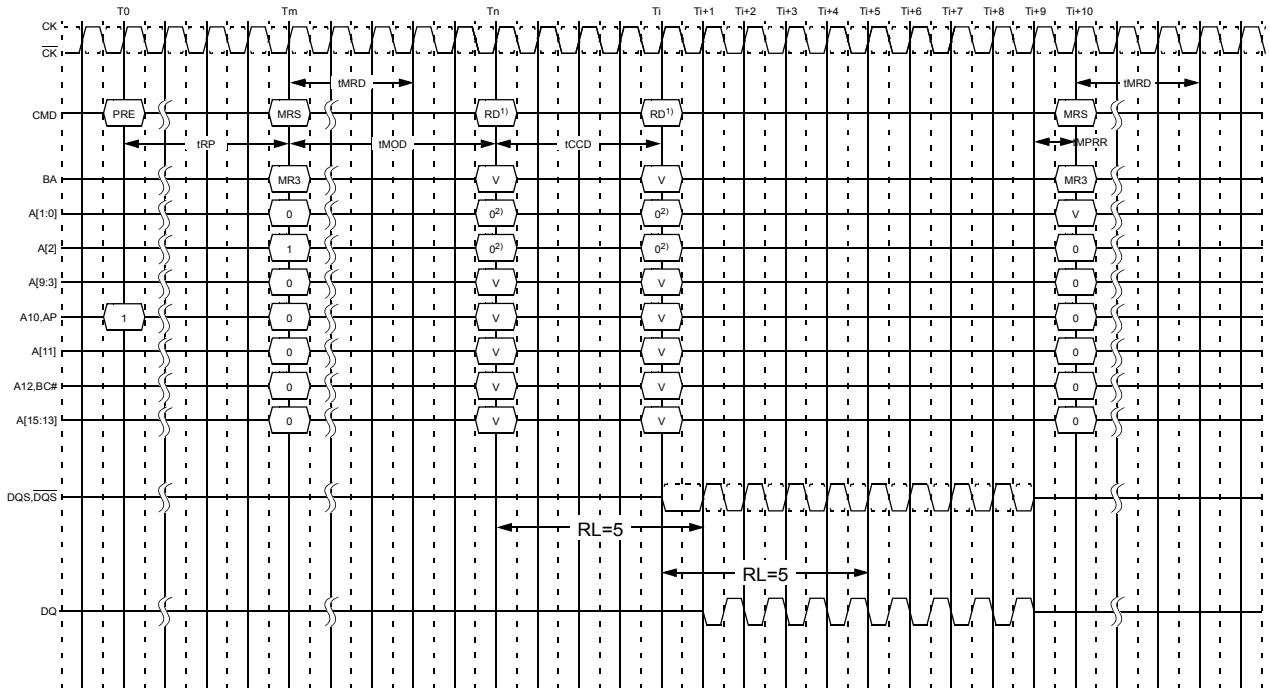
(RL=5tCK, Fixed Burst order and Single Readout)



Notes :
1) RD with BL8 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]

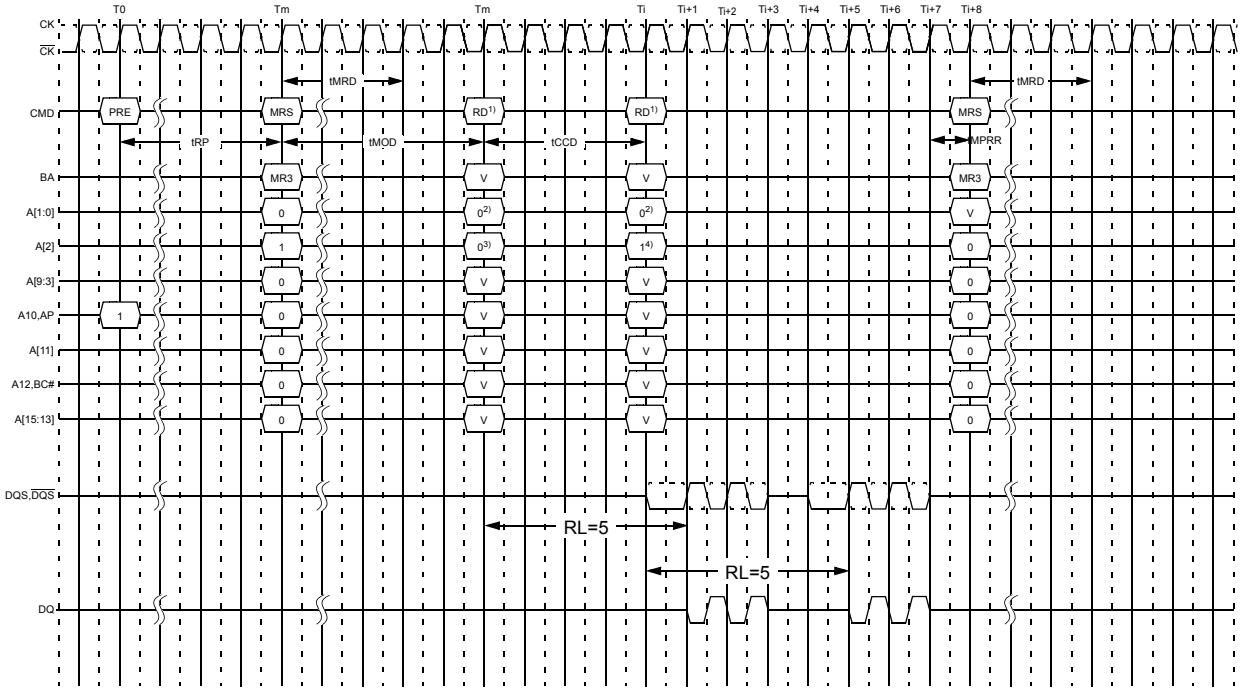
Readout of predefined pattern for system read calibration with BL8

(RL=5tCK, Fixed Burst order and Back-to-Back Readout)



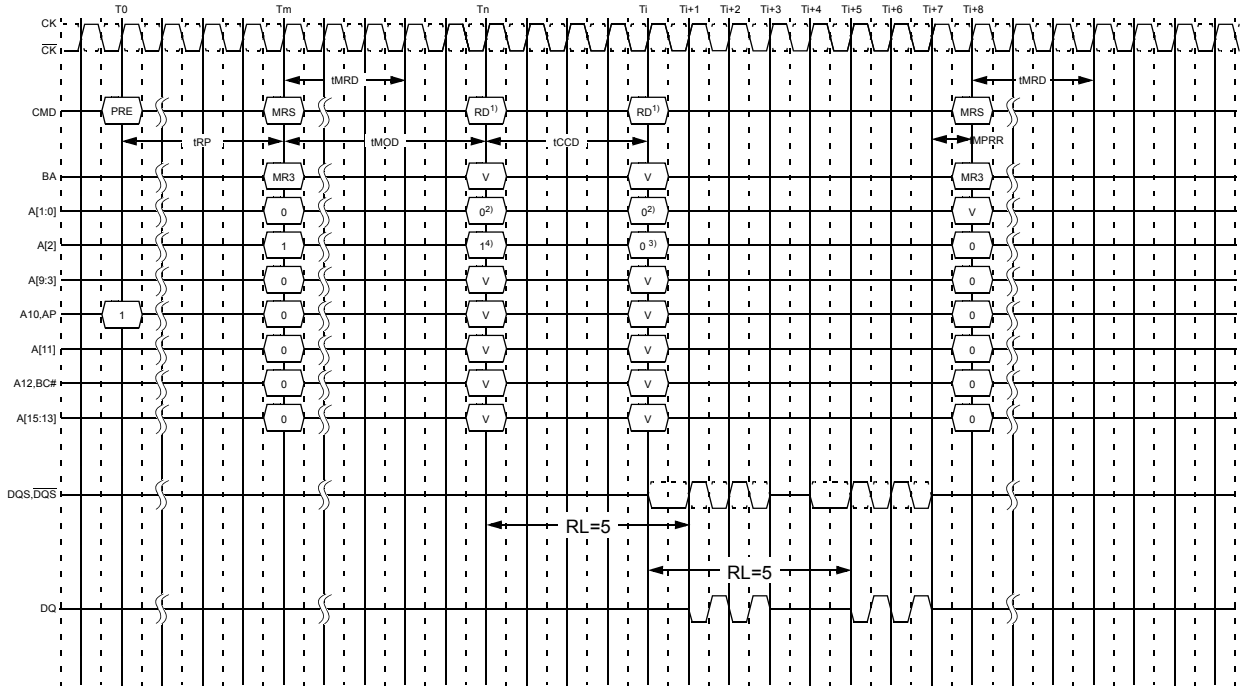
Notes :
1) RD with BL8 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]

Readout of predefined pattern for system read calibration with BC4
(RL=5tCK, First Lower Nibble then Upper Nibble)



Notes :
1) RD with BL8 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]
3) A[2]=0 selects lower 4 nibble bits 0...3
4) A[2]=1 selects upper 4 nibble bits 4...7

Readout of predefined pattern for system read calibration with BC4
(RL=5tCK, First Upper Nibble then Lower Nibble)

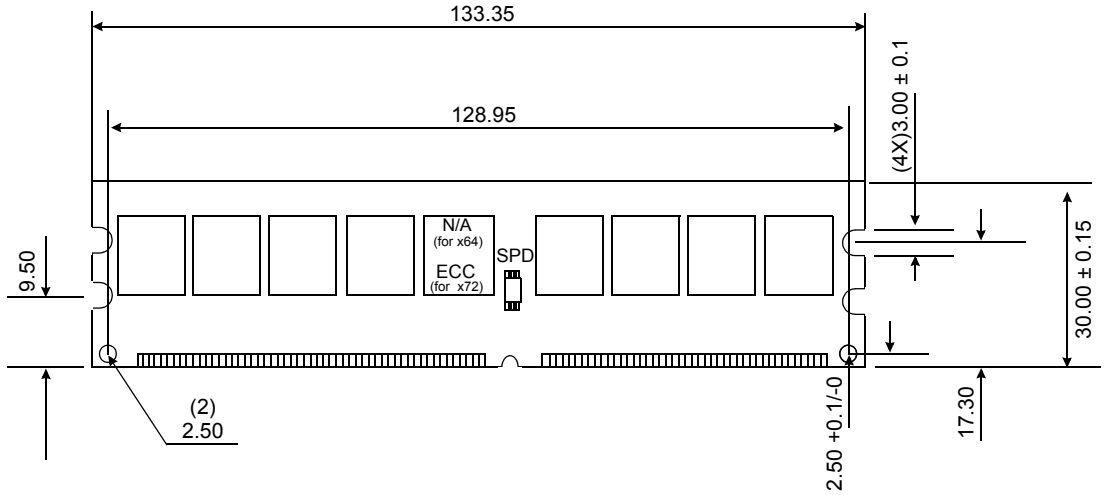


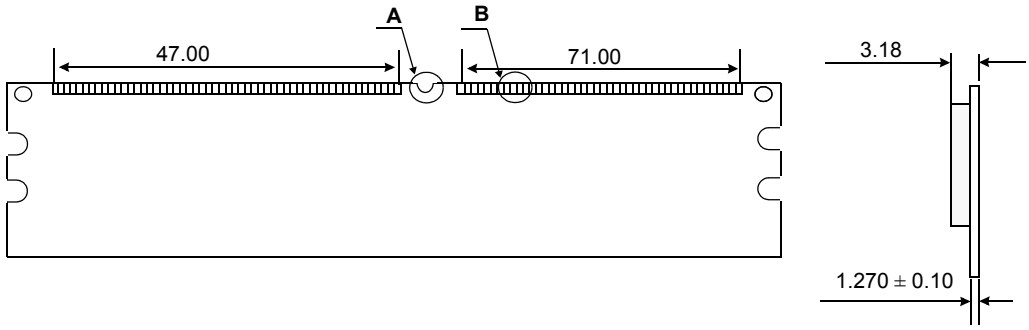
Notes :
1) RD with BL8 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]
3) A[2]=0 selects lower 4 nibble bits 0...3
4) A[2]=1 selects upper 4 nibble bits 4...7

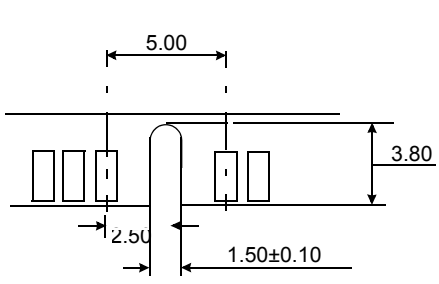
14.0 Physical Dimensions :

14.1 64Mbx8 based 64Mx64/x72 Module(1 Rank)

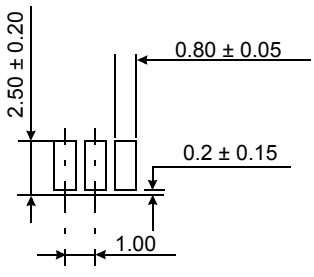
Units : Millimeters



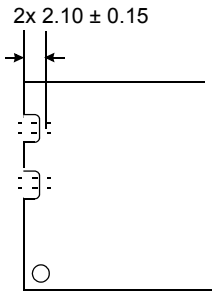




Detail A



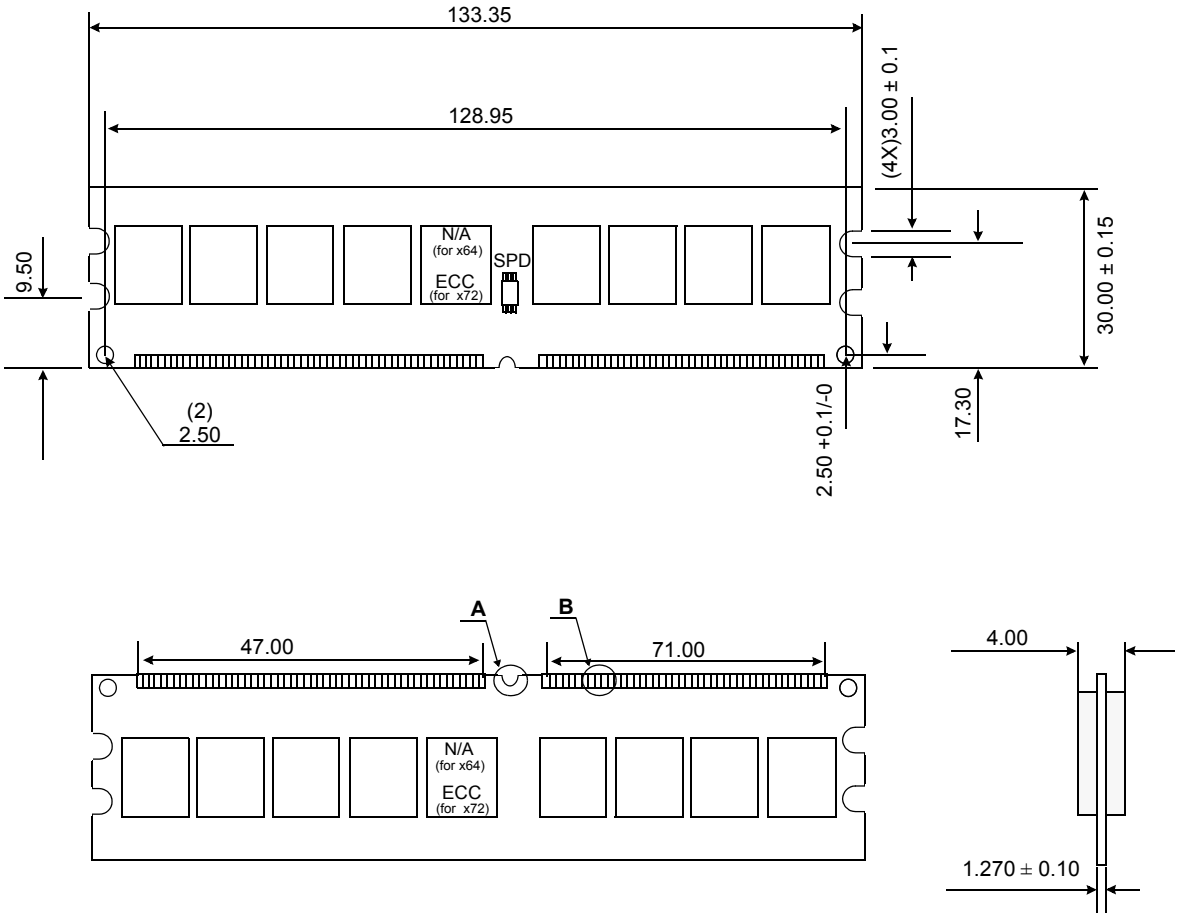
Detail B



The used device is 64M x8 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO :

14.2 64Mbx8 based 128Mx64/x72 Module(2 Ranks)

Units : Millimeters



Detail A **Detail B**

The used device is 64M x8 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO :